



Four Port Gigabit PMC Adapter Two Port Gigabit PMC Adapter

***OSS-IanPMC-4GC
OSS-IanPMC-2GC***

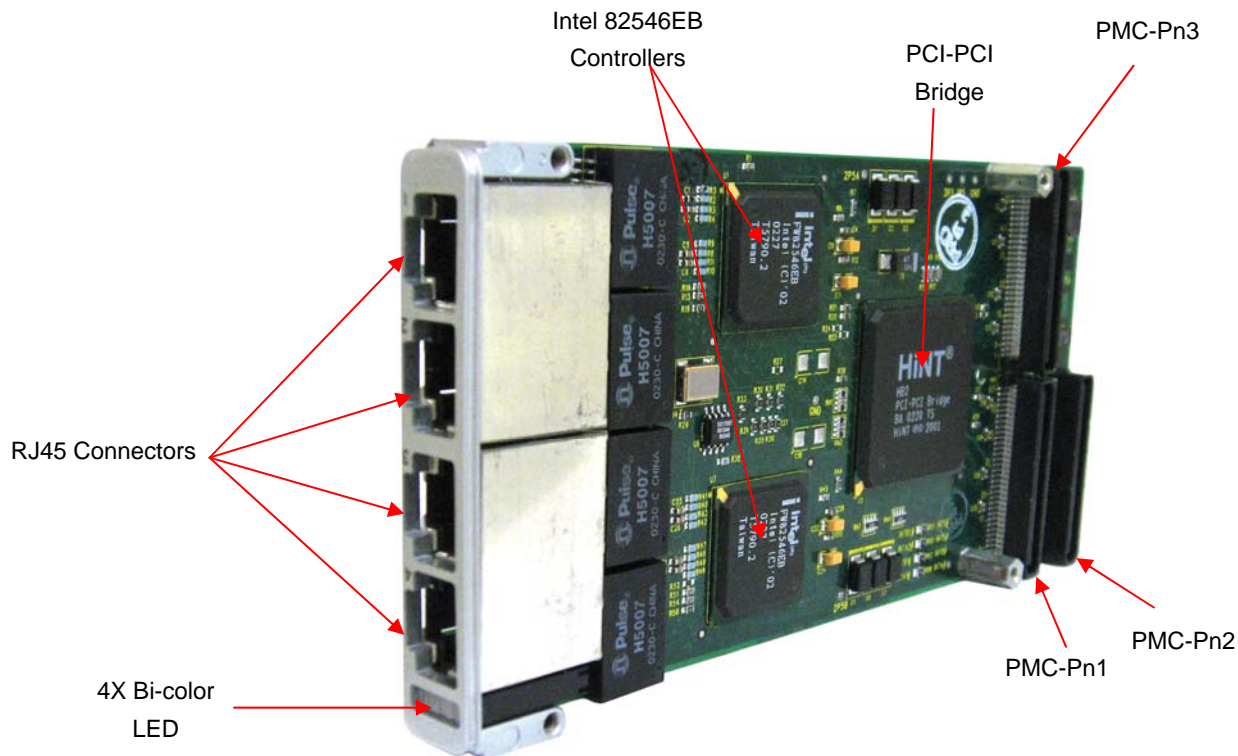


www.onestopsystems.com

Phone 877-438-2724 • Fax 760-466-1678 • sales@onestopsystems.com

Description

The OSS-lanPMC-4GC is a four port (Quad) Gigabit Ethernet over Copper PMC module. This design facilitates a computer system to communicate via four Ethernet ports at 10/100/1000 Mbit/sec rate. Attached to the OSS-lanPMC-4GC PCB is a PMC bezel with a custom stamp out to accommodate four RJ45 modular connectors and four bi-color LEDs. The OSS-lanPMC-4GC offers four ports of either 1000, 100 or 10 MHz connectivity providing clear-channel communication. Frames are transferred between the GigE ports and a 33/66-MHz, 64-bit host PCI bus.



Initial Set-Up

Unpacking Instructions

1. If the carton is damaged when you receive it, request that the carrier's agent be present when you unpack and inspect the equipment.
2. After unpacking, verify that all items listed in the packing list are present.
3. Inspect the equipment for shipping damage.
4. Save all packing material for storage or return shipment of the equipment.
5. For repairs or replacement of equipment damaged during shipment, contact One Stop Systems, Inc. to obtain a Return Materials Authorization (RMA) number and further shipping instructions.

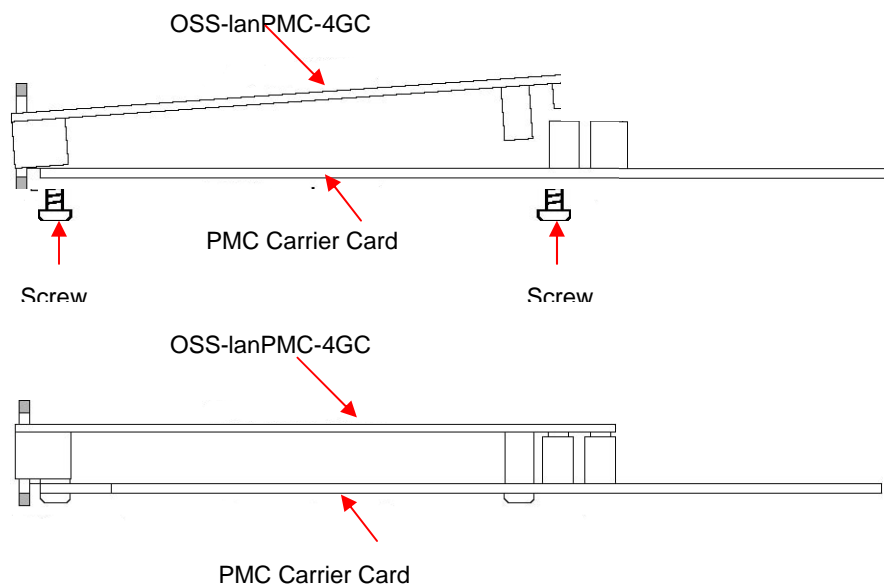
Installation and Removal

1. Power down the host system.
2. Open the chassis according to your system documentation.
3. Let the power supply cool down, if necessary.
4. Remove the host board from the system.
5. Remove the OSS-OSS-IanPMC-4GC from the protective bag, observing proper ESD safety procedures.

Installing the OSS-IanPMC-4GC:

1. Press the OSS-OSS-IanPMC-4GC bezel into the cutout in the PTMC carrier I/O panel. The gasket around the OSS-OSS-IanPMC-4GC bezel makes a tight fit to ensure an electromagnetic seal. Check that the bezel and gasket are pressed firmly into the carrier I/O.
2. Press the OSS-OSS-IanPMC-4GC down onto the carrier so PN1–PN3 plug into JN1–JN3 on the PMC carrier.
3. Install four screws to secure the board in place

Installation Diagram

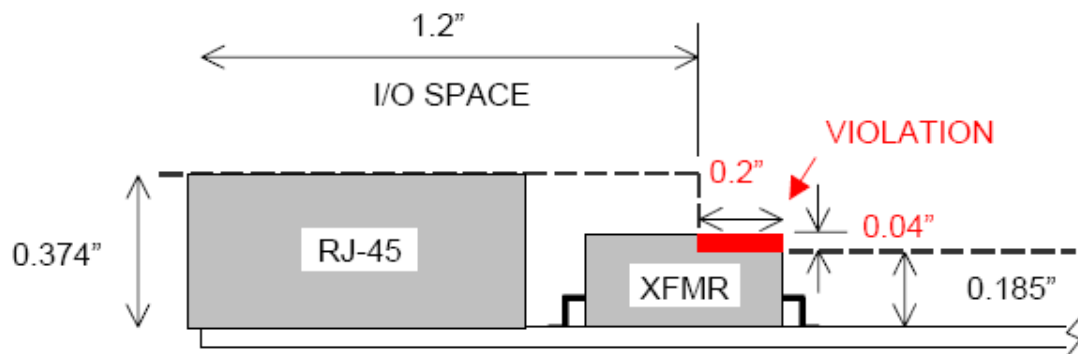


Specifications

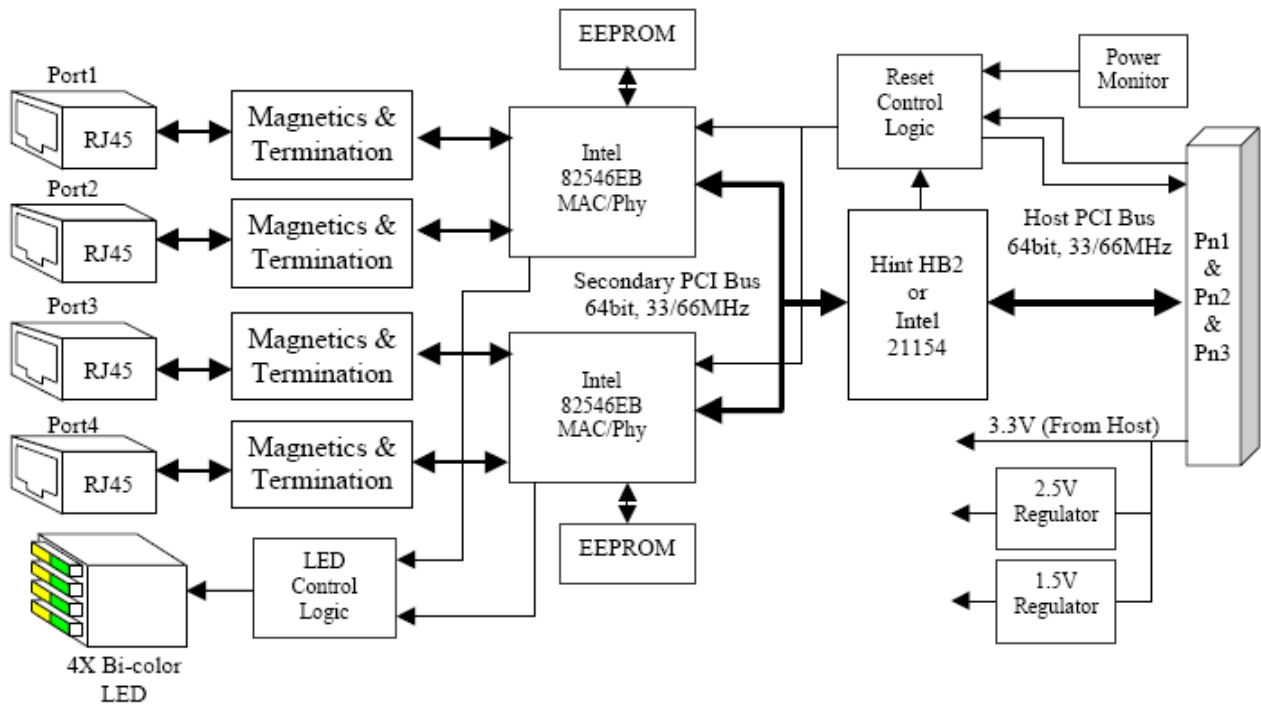
Electrical/Mechanical Specifications	
Form Factor:	64 bit, 33/66 MHz PMC interface (PCI Rev 2.2), 3.3V Signaling, 5V tolerant
Dimensions (H x L):	5.86 x 2.91 inches (148.8 x 73.9mm) (See component height section below)
Front Panel Connectors:	Four RJ45 connectors
Front Panel Indicators:	4X Bi-color LED
Power Consumption (designed to meet the following conditions)	
	9.48W typical @ 3.3V [Note that this is higher than the 7.5W PMC specification]
Operating Environment (designed to meet the following conditions)	
Temperature Range:	-5° to 55°C (23° to 136°F)
Relative Humidity:	20 to 80% non-condensing
Shock:	30g acceleration peak (11 ms pulse)
Vibration:	5-17 Hz 0.5" double amplitude displacement; 7-2000Hz, 1.5g acceleration.
Agency Compliance Designed to meet, but not tested	
	Pending

Component Height

Due to the density of the OSS-IanPMC-4GC design it is not possible to conform to the PMC component height restrictions. The height envelop (dotted line in the Figure) will be violated by approximately 0.040" next to the I/O space



Block Diagram



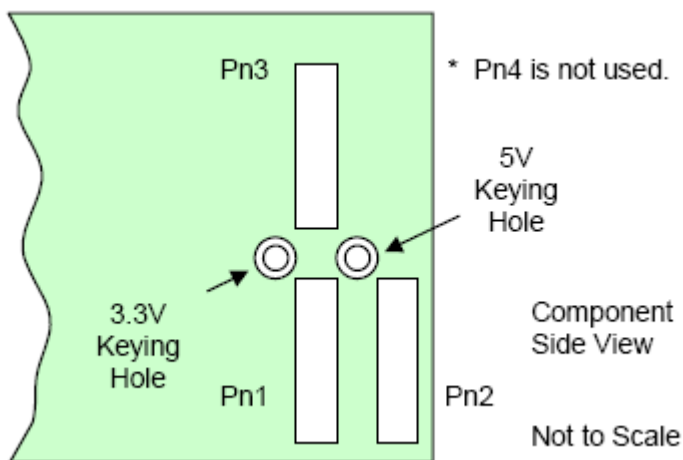
Busmode Pins

Since OSS-OSS-lanPMC-4GC supports only the PCI bus protocol at the PMC connectors, the BUSMODE1# pin is asserted LOW for two reasons only; (1) to indicate its presence to the host, and (2) to indicate that it is capable of performing PCI Bus protocol (see Table 5 below). The OSS-OSS-lanPMC-4GC responds within ten PCI clock cycles after detecting the state of BUSMODE[4:2]# pins.

BUSMODE[4:2]# state (input)	Mode	BUSMODE1# output state	Response explanation
000	"Card Present" test.	0	"Card Present" mode. No bus protocol is used and card is held in reset
001	Return Card Present if PCI capable and uses PCI protocol.	0	Capable of performing PCI protocol.
All other states	-	1	Card held in reset.

PMC Voltage Keying

The PCI-to-PCI bridge is capable of operating in either 3.3-volt or 5-volt signaling environments. Therefore, both voltage keying holes are provided on the PCB as shown below. When installing the card on a host, the voltage coding key (on the host) must be inserted in accordance with the host requirements. Note that 66MHz operation is only defined for 3.3-volt signaling.



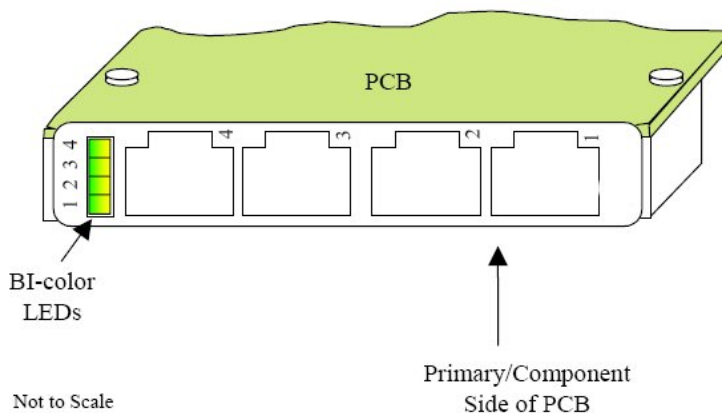
Ethernet Controller

Intel 82546EB is a Dual Port Gigabit Ethernet Controller in a single, compact component with two fully integrated Gigabit Ethernet MAC and PHY functions. The controller is capable of transmitting and receiving two channels of data at rates of 1000 Mbps, 100 Mbps, or 10 Mbps. It has a 64-bit wide PCI 2.2 compliant interface capable of operating at up to 66MHz (PCI-X 133MHz though supported by the device is not supported on this design). The device is in a 364 ball 1mm pitch BGA package. Two of these devices are used to implement the four ports of 10/100/1000BASE-T

The 82546EB have a System Management Bus (SMB) interface and Serializer/Deserializer interface. These interfaces are not used on lanPMC-4GC.

LEDs

There is a 4X Bi-color LED on the front, with one LED for each port. When a LINK is asserted the green LED will be turned on. When there is activity the yellow LED will be turned on. If there are continuous periods of activity, the green and yellow LEDs will alternate.



Connectors (continued)

Communication on the host PCI bus is done across two PMC connectors, **Pn1** and **Pn2**.

The OSS-OSS-IanPMC-4GC can use the **Pn4** connector for rear I/O.

Pn1 32-bit PCI				Pn2 32-bit PCI				Pn3 64-bit PCI			
Pin #	Name	Name	Pin #	Pin #	Name	Name	Pin #	Pin #	Name	Name	Pin #
1	TCK	-12V	2	1	+12V	TRST#	2	1	PCI-RSVD	Ground	2
3	Ground	INTA#	4	3	TMS	TDO	4	3	Ground	C/BE[7]#	4
5	INTB#	INTC#	6	5	TDI	Ground	6	5	C/BE[6]#	C/BE[5]#	6
7	BUSMODE1#	+5V	8	7	Ground	PCI-RSVD	8	7	C/BE[4]#	Ground	8
9	INTD#	PCI-RSVD	10	9	PCI-RSVD	PCI-RSVD	10	9	V(I/O)	PAR64	10
11	Ground	3.3Vaux	12	11	BUSMODE2#	+3.3V	12	11	AD[63]	AD[62]	12
13	CLK	Ground	14	13	RST#	BUSMODE3#	14	13	AD[61]	Ground	14
15	Ground	GNT#	16	15	+3.3V	BUSMODE4#	16	15	Ground	AD[60]	16
17	REQ#	+5V	18	17	PME#	Ground	18	17	AD[59]	AD[58]	18
19	V(I/O)	AD[31]	20	19	AD[30]	AD[29]	20	19	AD[57]	Ground	20
21	AD[28]	AD[27]	22	21	Ground	AD[26]	22	21	V(I/O)	AD[56]	22
23	AD[25]	Ground	24	23	AD[24]	+3.3V	24	23	AD[55]	AD[56]	24
25	Ground	C/BE[3]#	26	25	IDSEL	AD[23]	26	25	AD[53]	Ground	26
27	AD[22]	AD[21]	28	27	+3.3V	AD[20]	28	27	Ground	AD[52]	28
29	AD[19]	+5V	30	29	AD[18]	Ground	30	29	AD[51]	AD[50]	30
31	V(I/O)	AD[17]	32	31	AD[16]	C/BE[2]#	32	31	AD[49]	Ground	32
33	FRAME#	Ground	34	33	Ground	PMC-RSVD	34	33	Ground	AD[48]	34
35	Ground	IRDY#	36	35	TRDY#	+3.3V	36	35	AD[47]	AD[46]	36
37	DEVSEL#	+5V	38	37	Ground	STOP#	38	37	AD[45]	Ground	38
39	Ground	LOCK#	40	39	PERR#	Ground	40	39	V(I/O)	AD[44]	40
41	PCI-RSDV	PCI-RSVD	42	41	+3.3V	SERR#	42	41	AD[43]	AD[42]	42
43	PAR	Ground	44	43	C/BE[1]#	Ground	44	43	AD[41]	Ground	44
45	V(I/O)	AD[15]	46	45	AD[14]	AD[13]	46	45	Ground	AD[40]	46
47	AD[12]	AD[11]	48	47	M66EN	AD[10]	48	47	AD[39]	AD[38]	48
49	AD[09]	+5V	50	49	AD[08]	+3.3V	50	49	AD[37]	Ground	50
51	Ground	C/BE[0]#	52	51	AD[07]	PMC-RSVD	52	51	Ground	AD[36]	52
53	AD[06]	AD[05]	54	53	+3.3V	PMC-RSVD	54	53	AD[35]	AD[34]	54
55	AD[04]	Ground	56	55	PMC-RSVD	Ground	56	55	AD[33]	Ground	56
57	V(I/O)	AD[03]	58	57	PMC-RSVD	PMC-RSVD	58	57	V(I/O)	AD[32]	58
59	AD[02]	AD[01]	60	59	Ground	PMC-RSVD	60	59	PCI-RSVD	PCI-RSVD	60
61	AD[00]	+5V	62	61	ACK64#	+3.3V	62	61	PCI-RSVD	Ground	62
63	Ground	REQ64#	64	63	Ground	PMC-RSVD	64	63	Ground	PCI-RSVD	64

Technical Reference

Host PCI Bus Interface

The OSS-lanPMC-4GC is designed to accommodate the HiINT HB2 or Intel 21154BE PCI-to-PCI bridge. This device is packaged in a 304 ball PBGA package. It is capable of 64bit, 33/66MHz operation in 3.3V and 5V signaling (33MHz only) environments. The two Ethernet Controllers are attached to the secondary side of this bridge, however, the interrupt lines from the Controllers are wired directly to the PMC connectors. Each Controller has two interrupt outputs, one for each port

Device	Device #	IDSEL	Device INTA#	Device INTB#
Ethernet Controller Ports 1&2	4	S_AD20	PMC/PCI INTA#	PMC/PCI INTB#
Ethernet Controller Ports 3&4	6	S_AD22	PMC/PCI INTC#	PMC/PCI INTD#

Provision is made for Ethernet Controller for Ports 3&4 to use interrupts to INTA# and INTB# instead of INTC# and INTD# (resistor stuffing option) by change the device number to 8 by using S_AD24 instead of S_AD22. In this case both devices will use INTA# and INTB#.

Note: The secondary PCI Bus will operate at the same frequency as the host PCI bus. HB2 can operate secondary bus at 66MHz when the Host bus is operating at 33MHz by using an external oscillator. This feature is not implemented to maintain compatibility with 21154EB and to reduce complexity.

EEPROM

OSS-lanPMC-4GC uses one 256x16 EEPROM for each 82546EB Ethernet Controller. The 256x16 device is required for supporting altering applications (ASF). For non-altering applications a 64x16 device may be used. By default the OSS-lanPMC-4GC uses the 256x16 device, however, the ASF functionality is not enabled.

ST Microelectronic's M93C66WMN6 and Atmel's AT93C66-10SI-2.7 are two suitable 256x16 Serial Microwire devices compatible with the 82546EB

EEPROM Address Map

Word	Used By	Bit 15-8	Bit 7-0	Image Value	LAN A/B
0x00	HW *	Ethernet Address Byte 2	Ethernet Address Byte 1	IA(2,1)	both
0x01		Ethernet Address Byte 4	Ethernet Address Byte 3	IA(4,3)	
0x02		Ethernet Address Byte 6	Ethernet Address Byte 5	IA(6,5)	
0x03	SW	Compatibility High	Compatibility Low	0x0000	both
0x04				0x0000	
0x05				0x0000	
0x06				0x0000	
0x07				0x0000	
0x08	SW *	Board Revision (OSS Custom)		Assy	
0x09	SW *	Interface Type (OSS Custom)		Assy	

EEPROM (continued)

EEPROM Address Map(continued)

Word	Used By	Bit 15-8	Bit 7-0	Image Value	LAN A/B
0x0A	HW	Init Control 1		both	
0x0B	HW	Subsystem ID (High, Low)	0x0802	both	
0x0C	HW	Subsystem Vendor ID (High, Low)	0x1176	both	
0x0D	HW	Device ID (High, Low)	0x1010	LAN A	
0x0E	HW	Vendor ID (High, Low)	0x8086	both	
0x0F	HW	Init Control 2		both	
0x10	HW	Software Defined Pins Control	0xXXXX	LAN B	
0x11	HW	Device ID (High, Low)	0x1010	LAN B	
0x12	HW		Common Power		both
0x13	HW	Management Control		LAN B	
0x14	HW	Init Control 3	SMBus Address	0xXXXX	LAN B
0x15 0x16	HW	IPv4 Address Byte 2 IPv4 Address Byte 4	IPv4 Address Byte 1 IPv4 Address Byte 3	IP(2,1) IP(4,3)	LAN B
0x17 0x18 0x19 0x1A 0x1B 0x1C 0x1D 0x1E	HW	IPv6 Address Byte 2 IPv6 Address Byte 4 IPv6 Address Byte 6 IPv6 Address Byte 8 IPv6 Address Byte 10 IPv6 Address Byte 12 IPv6 Address Byte 14 IPv6 Address Byte 16	IPv6 Address Byte 1 IPv6 Address Byte 3 IPv6 Address Byte 5 IPv6 Address Byte 7 IPv6 Address Byte 9 IPv6 Address Byte 11 IPv6 Address Byte 13 IPv6 Address Byte 15	IP(2,1) IP(4,3) IP(6,5) IP(8,7) IP(10,9) IP(12,11) IP(14,13) IP(16,15)	LAN B
0x1F		Reserved	Reserved		
0x20	HW	Software Defined Pins Control	0xXXXX	LAN A	
0x21	HW	Circuit Control	0x7861	both	
0x22	HW	D0 Power	D3 Power	0x280C	both
0x23	HW	Management Control	0xXC8	LAN A	
0x24	HW	Init Control 3	SMBus Address	0xXXXX	LAN A
0x25 0x26	HW	IPv4 Address Byte 2 IPv4 Address Byte 4	IPv4 Address Byte 1 IPv4 Address Byte 3	IP(2,1) IP(4,3)	LAN A
0x27 0x28 0x29 0x2A 0x2B 0x2C 0x2D 0x2E	HW	IPv6 Address Byte 2 IPv6 Address Byte 4 IPv6 Address Byte 6 IPv6 Address Byte 8 IPv6 Address Byte 10 IPv6 Address Byte 12 IPv6 Address Byte 14 IPv6 Address Byte 16	IPv6 Address Byte 1 IPv6 Address Byte 3 IPv6 Address Byte 5 IPv6 Address Byte 7 IPv6 Address Byte 9 IPv6 Address Byte 11 IPv6 Address Byte 13 IPv6 Address Byte 15	IP(2,1) IP(4,3) IP(6,5) IP(8,7) IP(10,9) IP(12,11) IP(14,13) IP(16,15)	LAN A
0x2F	HW	LEDCTL Default	0x0602	both	
0x30 0x31 0x32 0x33 0x34 ... 0x3E	PXE	PXE Word 0 (Software Use) Config PXE Word 1 (Software Use) Config PXE Word (Software Use) PXE Version PXE Word (Software Use) EFI Version PXE Word ... PXE Word			
0x3F	*	Software Checksum, words 0x00 through 0x3F			
0x40 ... 0xF7	ASF	See 8245EB Developer's Manual			
0xF8 ... 0xFD	SW	Reserved for future OSS use.	0x0000		
0xFE 0xFF	SW	Free for Application Use	0x0000		

Ethernet Address

The Ethernet Individual Address (IA) is a 6 byte field (IA1:IA2:IA3:IA4:IA5:IA6) that must be unique for each Ethernet port (and unique for each copy of the EEPROM image). The first three bytes (IA1-IA3) are vendor specific. The value from this field is loaded into the Receive Address Register 0 (RAL0/RAH0).

Since the 82546EB is a dual-port device, the Ethernet Address in these words will be assigned to LAN A. The Ethernet Address for LAN B is the Ethernet Address for LAN A + 1.

In the past OSS has used the 6 digit binary coded board serial number (3 bytes or 6 nibbles long) as the port specific portion of the MAC address. For example, if the board serial number is 123456 the MAC address becomes 00:a0:d6:12:34:56. In cases where there are multiple Ethernet Ports on a card the first port is assigned its address in this way. The remaining ports use the board serial number in hexadecimal (becomes 5 nibbles) together with hexadecimal digits A through F for the sixth nibble as the address, thus enabling up to 7 ports on each board.

Since the 82546EB automatically assigns the address for port B by adding 1 to the address of the port A the addressing scheme needs to be modified slightly. The following scheme will be used:

On a four port board with board serial number 123456 port 1 (port A of Ethernet Controller 1) will be assigned address 00:60:99:1E:24:0A, where 006099 is vendor ID for OSS's LAN products. 1E240 is the board serial number in hexadecimal and A corresponds to port 1. Ethernet Controller will automatically make the address for port 2 (its port B) 00:60:99:1E:24:0B by adding 1 to its port A address. The port 3 (port A Ethernet Controller 2) will be assigned address 00:60:99:1E:24:0C, where 1E240 is the board in hexadecimal and C corresponds to port 3. Ethernet Controller will automatically make the address for port 4 (its port B) 00:60:99:1E:24:0D by adding 1 to its port A address. The least significant nibble of MAC address on OSS-lanPMC-4GC will always be a hexadecimal digit (A, B, C, or D).

Note that the most significant byte of MAC address is stored at bits 7-0 of word zero. For example, if the MAC address is 01:02:03:04:05:06 the Ethernet address will be stored as-

Word	Bit 15-8	Bit 7-0
0x00	2	1
0x01	4	3
0x02	6	5

Board Revision & Interface Type

Words 0x08 & 0x09 are used by Intel to store their nine-digit assembly number. These words are available to hardware manufacturer to use as appropriate. On OSS-lanPMC-4GC these two words are used for storing for Board Revision (0x08) and Interface Type (0x09). The driver or application may use these fields to get additional information about the card. The meaning of bits in these words is described on the next page :

Board Revision:

This word specifies the board assembly revision. The contents of this word will correspond to the revision marked on the PCB.

Bit 15	Bits 14-8	Bits 7-0
IWI	BRM[6:0]	BRP[7:0]

IWI	Interface Word Invalid	0	Use Word 0x09 to determine Interface Type
		1	Word 0x09 is invalid Use 0xF8 through 0xFD for additional information about the card (Implementation TBD)
BRN[6:0]	Board Revision Main		Assembly's Main Revision
BRP[7:0]	Board Revision Point		Assembly's Minor Revision Number
			Eg., for board revision 2.1 BRM will be 0x2 and BRP will be 0x1

Interface Type:

This word gives information about the type of media (copper or optical) and type of connectors etc. The bits in this word are designated according to anticipated future requirements. The following table shows the values for lanPMC-4GC. Note that bits 13-12 SHOULD NOT be used by driver or application to determine the number of ports. Instead, use number of PCI devices that have the same board serial number (determined from MAC address) to determine number of ports.

Bit 15	Bit 14	Bits 13-12	Bits 11-8	Bits 7-4	Bits 3-0
MEDIA	TAM	NP[1:0]	Reserved	Reserved	CT/IT[3:0]
0	0	00	0000	0000	0000

MEDIA	Type of Interface Media	0 Copper 1 Optical (lanPMC-4GF)
TAM	Type of Attachment Module	0 Fixed (Soldered to board) 1 Pluggable (e.g., SFP optical xceiver) IT[3:0] may not be valid
NP[1:0]	Reserved for Number of Ports (DO NOT USE THESE BITS TO DETERMINE NUMBER OF PORTS.)	These bit are reserved for future use. 00 Four Ports (Default for 4-port lanPMC-4GC) 01 One Port 10 Two Ports 11 Reserved
CT/IT[3:0]*	Connector Type or Interface Type	0x0 RJ-45 Other values are reserved for future use

* CT (connector type) applies to copper (lanPMC-4GC) and IT (interface type) applies to optical, e.g., 850 nm LC, or 1310 nm RJ, or 850 nm SC (lanPMC-4GF).

Subsystem ID

OSS-lanPMC-4GC is assigned subsystem ID 0x0802.. It is recommended that the subsystem ID for two-port and one-port versions of this product remain the same and other means be used to identify the number of ports (e.g., number of PCI devices that have the same board serial number).

Checksum Word Calculation

The Checksum word (0x3F) should be calculated such that after adding all the words (0x00-0x3F), including the Checksum word itself, the sum should be 0xBABA. The initial value in the 16-bit summing register should be 0x0000 and the carry bit should be ignored after each addition. This checksum is not accessed by the 82546EB device. If CRC checking is required, it must be performed by software.

Sample EEPROM Image File

Following is a sample of the EEPROM image file. The format is based on Intel's EEUPDATE utility.

Warning!!

Great care must be taken to ensure that words 0x0D and 0x0F are not changed from 1010 and 8086 respectively as changing them could make the device inaccessible.

```
; *****
; * CuGeR EEPROM IMAGE FILE FOR 82546 *
; * DOCUMENT NUMBER: 9034-42_2 *
; * DOCUMENT REVISION: 2 *
; * FOR BOARD: JNVF5302 REV 2 *
; *****
; THIS FILE CONFORMS TO THE REQUIREMENTS FOR INTEL EEUPDATE
; UTILITY AND IS FOR A 256 WORD DEVICE (E.G., 93C66).
;
; THE BOARD REVISION FIELD (0X08) MUST BE CHANGED EVERY TIME
; THERE IS A BOM CHANGE AND THE REVISION OF ASSEMBLY CHANGES.
;
; SEE BOTTOM OF THIS FILE FOR NOTES AND REVISION LOG.
;
; CURRENT DATA
; BOARD REVISION (0X08) = 0200
; INTERFACE TYPE (0x09) = 0000
; SUBSYSTEM ID (0X0B) = 0802
; OSS VENDOR ID (0X0C) = 1176
;
;0/8 1/9 2/A 3/B 4/C 5/D 6/E 7/F
DEAD DEAD DEAD 0430 FFFF FFFF FFFF FFFF
0200 0000 460A 0802 1176 1010 8086 3428 ;0 <-- BOARD REV AT 0X08
C300 1010 0000 2100 1800 FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF 0000 ;1
C300 7861 280C 2100 0800 FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF 0602 ;2
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF DEAD ;3
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF ;4
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF ;5
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF ;6
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF ;7
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
```

```

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF ;8
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF ;9
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF ;A
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF ;B
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF ;C
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF ;D
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF ;E
FFFF FFFF FFFF FFFF FFFF FFFF FFFF DEAD
0000 0000 0000 0000 0000 0000 0000 0000 ;F
; -----

```

REVISION LOG

```

;
; REV 2: 01-14-2003 (AM)
; CHANGED BIT 0 OF WORD 0X0A TO 0 FROM 1 TO PREVENT LOADING OF
; VENDOR/DEVICE ID. 82546 AUTOMATICALLY ASSIGNS 8060 & 1010.
;
; NOTES:
; BOARD REVISION IS SPECIFIED AT WORD 0X08 AS FOLLOWS:
; BITS [15:8] REPRESENT THE SIGNIFICANT (MAJOR) REVISION AND
; BITS [7:0] REPRESENT THE SUB (MINOR) REVISION.
; E.G.,
; JNVF5302 REV 2 IS SPECIFIED AS 0200
; JNVF5302 REV 2.1 IS SPECIFIED AS 0201

```

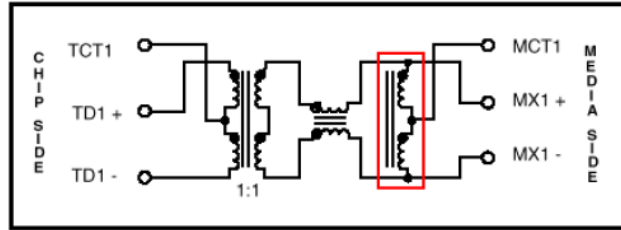
```

THE BOARD REVISION FIELD MUST BE CHANGED EVERY TIME THERE
; IS A BOM CHANGE AND THE REVISION OF ASSEMBLY CHANGES.
;
; *** END OF FILE ***

```

Magnetics

The 82546EB requires a 1:1 transformer with chip and media side center taps and a common mode choke. Per Intel, the media side center tap must be via an auto transformer. Figure 2 shows this structure for one pair of media wires. The magnetic module will have four such structures for the four media pairs. The auto transformers are identified by a box around them



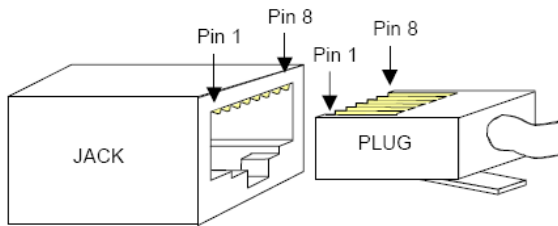
One magnetic module is used per port on the lanPMC-4GC. This enables depopulation of devices to achieve single port version.

Due to the density of OSS-lanPMC-4GC design (four ports) it is not possible to comply with the CMC component height requirement. The transformer modules encroach the standard component height area by 0.2" and violate the maximum height requirement by 0.04

RJ-45

Two dual-port shielded compact ganged CAT-5 jacks from Molex (P/N 445600022) are used to implement the physical media attachment (PMA) for the four ports.

The assignment of 1000BASE-T PMA signals is shown in the table below, and the figure below shows the Pin 1 reference for the Plug and the Jack. Note that only pins 1 & 2 (Tx) and 3&6 (Rx) are used for the 10Mbps and 100Mbps application. Refer to sections 14.5 and 40.8 (reference 17) of IEEE 802.3 for additional information.



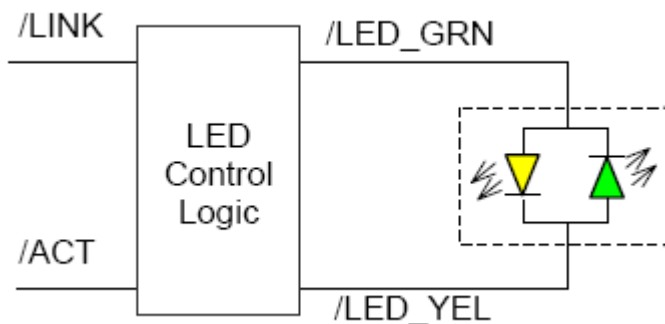
Contact (Pin)	MDI Signal (OSS-lanPMC-4GC Jack)	MDI-X Signal(cross-over)
1	BI_DA+	BI_DB+
2	BI_DA-	BI_DB-
3	BI_DB+	BI_DA+
4	BI_DC+	BI_DD+
5	BI_DC-	BI_DD-
6	BI_DB-	BI_DA-
7	BI_DD+	BI_DC+
8	BI_DD-	BI_DC-

LEDs

The 82546EB has four signals per port designated to control LEDs. Since there is only limited space to put LEDs on the lanPMC-4GC, only LEDs to indicate link and activity are provided. A four-high stacked bi-color LED visible from front panel is used to indicate link and activity status. One LED is assigned to each port.

Note: The LED configuration should be left at default values for proper operation of LEDs on lanPMC-4GC. That is, LED0=LINK_UP, LED1=blinking ACTIVITY, LED2=LINK_100 (don't care on lanPMC-4GC), and LED3=LINK_1000 (not used on lanPMC-4GC). See section 6.3.0.19, Chapter 11, and section 14.4.14 of 82546EB Developers Manual, Rev. 0.25 for definition of LED0-LED3 and for additional information. If any changes are to be made to the LED configuration, carefully consider the impact to implementation of LED control described below.

Since the bi-color LED is configured back to back (see Figure 4) and active low outputs are assumed from 82546EB (default configuration), external logic is used to control the LED. The LED operation is as follows: when the LINK is asserted (LINK_UP) the Green LED is turned on; when the ACT signal is asserted (note that the LINK will remain low by default configuration) the Yellow LED is turned on.



/LINK	/ACT	/LED_GRN	/LED_YEL	Comment
1	1	1	1	Both LEDs off
0	1	0	1	Green LED on
X	0	1	0	Yellow LED on

If there are continuous periods of activity, the green and yellow LEDs will alternate.

Note that regardless of the numbers of ports (4, 2, or 1), four LEDs will always be visible from the front panel, but only the LED(s) corresponding port(s) present will be functional.

In addition to the port status LEDs there is a yellow LED, not visible from the front panel, that is illuminated when the module is in a reset stat.

The LED control logic is implemented in an EPM3032 CPLD together with the reset logic.

Note: Though not used to control any LEDs the LINK_1000 signals (LED3) from the 82546EB are connected to the CPLD for future use.

CPLD

An EPM3032A CPLD from Altera is used to implement the LED control and reset functions. There are no Host accessible registers in the CPLD. There are 30 user I/O pins of which all but one are used

Clocks

The 82546EB requires a 25MHz, +/- 50ppm clock. One 25MHz oscillator is used to supply clocking to both the Controllers

Power

OSS-IanPMC-4GC requires three voltages—3.3V; 2.5V, and 1.5V. The 2.5V and 1.5V are required by the Ethernet Controllers, while *all* the devices require 3.3V. Since this board is designed specifically for use in 66MHz systems (to achieve optimum performance), it can be assumed that the host will provide ample and clean 3.3V to the module. Anticipating that some systems may not provide 5V at all, or limit the amount of current available, 2.5V and 1.5V are regulated from the 3.3V. The following subsections discuss these in more detail.

Note: Under normal conditions OSS-IanPMC-4GC does not require 5V from the host. However, if the Intel 21154 is used, due to a device errata, its primary V (I/O) pin may need to be tied to 5V when operating at 66MHz in a 3.3V signaling environment. This only affects the biasing of the PCI I/O drivers and not the actual signaling level. The board is designed to accomplish this. Should this workaround be necessary, OSS-IanPMC-4GC will require 5V from the Host

Regulator – 1.5V

1.5V is required for 82546EB's core. Each device requires 840mA (Max.) for a total of 1.68A. A step-down switching regulator is implemented using Linear Technology's LTC1772B. As mentioned earlier, 3.3V is regulated down to 1.5V. The LTC1772B is packaged in a 6-lead SOT-23 package and requires an external P-MOSFET. The Si3443DV in a TSOP-6 package is selected as the P-MOSFET for this application.

Regulator – 2.5V

2.5V is also required by 82546EB for its operation. The current requirement is 480mA (Max.). To simplify the power supply design and distribute the load, each 82546EB is powered by its own 2.5V low-drop out (LDO) linear regulator. The regulator used is IRU1206 (or equivalent) in a SOT-223 package. This regulator can handle 1A and has a drop-out of 0.4V (Max.) at 500mA load allowing regulation with input as low as 2.9V

Protection

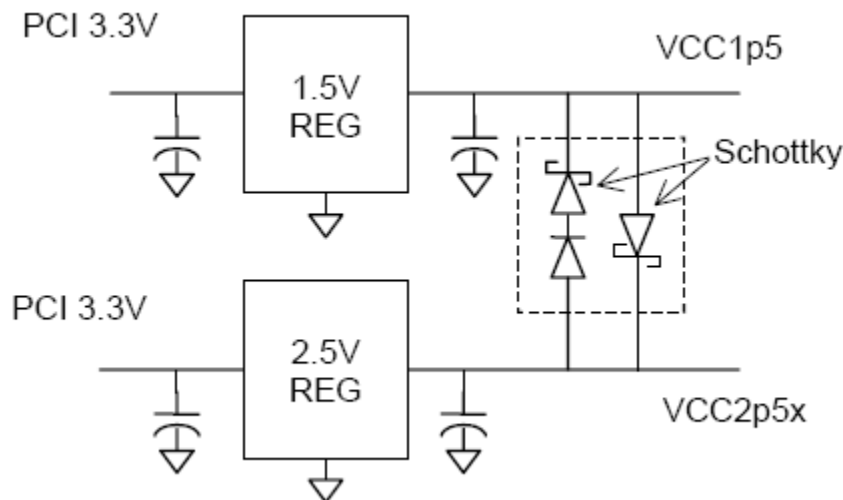
Since there are multiple devices providing power to the Ethernet Controllers a protection scheme is implemented so as to prevent excessive voltage difference between the various power pins.

Since the 2.5V is generated using a linear regulator it will essentially follow the 3.3V input and no voltage differences issues are anticipated between the 3.3V and 2.5V pins. The 1.5V on the other hand is generated using a switching regulator and can experience start-up delays or other problems such as power supply malfunction. The protection scheme used is shown in Figure 5. A series combination of a standard diode and a Schottky diode is connected between the 2.5V and 1.5V rails and a Schottky diode is connected from the 1.5V to 2.5V rail. Since we expect the 2.5V rail to follow the 3.3V rail, by having the protection diodes between the 1.5V and 2.5V rails we don't need to worry about differences between the 3.3V and the 1.5V rails.

Since there are two 2.5V regulators, one for each Ethernet Controller, the protection scheme is implemented for each 2.5V supply.

Protection (continued)

The “x” in VCC2p5x in the figure below represents A or B for the two 2.5V rails.



Power Monitor

A Dallas Semiconductor DS1706TESA in a SO-8 package is used to generate power-up reset and monitor the 3.3V and 1.5V rail. The 2.5V rails are not monitored since these are generated using linear regulators from 3.3V and the probability of field failure is low. Also, since there are two independent 2.5V rails, one for each Ethernet Controller, trying to sense them would add complexity and cost with minimal gain.

If either 3.3V or 1.5V is below its minimum level the DS1706 will assert its /RST output and the board will be placed in reset. The DS1706 also asserts its /RST output at power-up and keeps it asserted for about 150mS after the power has stabilized. This provides sufficient time for the 1.5V power rail to stabilize before the board operation commences.

Reset

The board is in reset if any one of the following conditions is true:

- PCI reset is asserted.
- BUSMODE[4:2]# don't correspond to PCI protocol. Note: If BUSMODE pins are not implemented properly on the host then lanPMC-4GE will not come out of reset. In such situations the CPLD may be modified to ignore the BUSMODE inputs.
- Reset output of DS1706 (power monitor) is asserted, i.e., either 3.3V or 1.5V is in under-voltage condition.

Note that when the OSS-lanPMC-4GC is in reset the Ethernet Controllers will not be accessible from the host. A **yellow** LED is provided to indicate the reset state of the board. Past experience has shown that this is a useful indicator for troubleshooting. The reset logic is implemented in an EPM3032 CPLD together with the LED control logic