

Multi Port T1/E1/J1 PCI Adapter

OSS-wanPCI-CxT1E1



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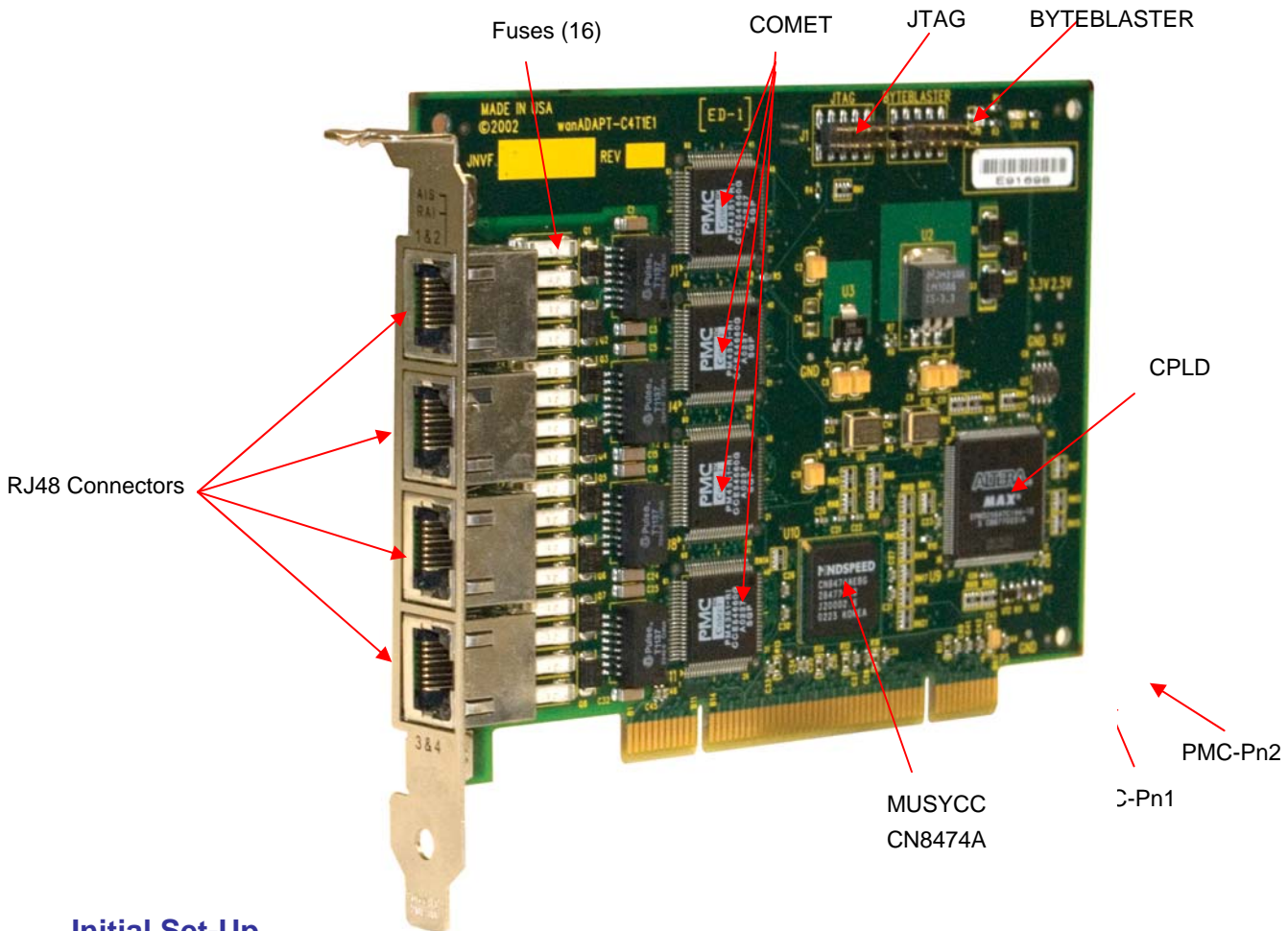
Description

The OSS-wanPCI-CxT1E1 products are adapters in PCI short card form factor:

- OSS- wanPCI-C1T1E1 (single port)
- OSS-wanPCI-C2T1E1 (dual port)
- OSS-wanPCI-C4T1E1 (quad port) [SHOWN BELOW]

Throughout this reference, the term wanADAPT-CxT1E1 is used to refer to all three adapters.

This design facilitates communication via one, two, or four ports (depending on the adapter) at T1/E1/J1 rates (1.544MHz, 2.048MHz, and 1.544MHz, respectively) with other types of systems. Channelized DS0 support is available for T1/E1 or J1. The OSS-wanPCI-CxT1E1 can use both SS7 or HDLC protocols..



Initial Set-Up

Unpacking Instructions

1. If the carton is damaged when you receive it, request that the carrier's agent be present when you unpack and inspect the equipment.
2. After unpacking, verify that all items listed in the packing list are present.
3. Inspect the equipment for shipping damage.
4. Save all packing material for storage or return shipment of the equipment.
5. For repairs or replacement of equipment damaged during shipment, contact One Stop Systems, Inc. to obtain a Return Materials Authorization (RMA) number and further shipping instructions.

Installation and Removal

1. Power down the host system.
2. Open the chassis according to your system documentation.
3. Let the power supply cool down, if necessary.
4. Remove the OSS-wanPCI-CxT1E1 from the protective bag, observing proper ESD safety procedures.

Installing the OSS-wanPCI-CxT1E1:

1. Insert the OSS-wanPCI-CxT1E1 in an open PCI slot. The adapter is a universal-keyed 32 bit board.
2. Make sure that the adapter is well seated and tighten the screw.
3. Close the chassis according to your system documentation
4. Attach the cable. Use an 8-position modular (RJ-48) straight-through patch cord to make the connection between the RJ-48 jack on the adapter and the RJ-48 jack in your wall or test system.
5. Turn on power to the computer. Adapter installation is complete.
6. Reverse the above procedure to remove the board

Specifications

Electrical/Mechanical Specifications	
Form Factor:	32-bit 33Mhz PCI 2.1 or PCI 2.2 Universal Key [5V or 3.3V]
Dimensions (H x L):	4.2 x 5.5 inches (106.7 x 139.7 mm)
Front Panel Connectors:	1,2 or 4 RJ48 connectors
Front Panel Indicators:	RAI and AIS LEDs on RJ48 connectors, Power LED
Operating Environment (designed to meet the following conditions)	
Temperature Range:	-5° to 55°C (23° to 136°F)
Relative Humidity:	20 to 80% non-condensing
Shock:	30g acceleration peak (11ms pulse)
Vibration:	5-17 Hz 0.5" double amplitude displacement; 7-2000Hz, 1.5g acceleration.
Agency Compliance Designed to meet, but not tested	
	Pending
MTBF (Telecordia TR-332 Version 6)	
	395,000 hours

Communications Controller

Conexant CN8474A communications controller

The OSS-wanPCI-CxT1E1 uses a Conexant CN8474A communications controller as the HDLC processing engine.

- The CN8474A Multichannel Synchronous Communications Controller (MUSYCC) is an advanced, multichannel, synchronous communications controller that formats and deformats 128 HDLC channels in a single CMOS IC.
- The MUSYCC provides HDLC channels for internetworking applications such as Frame Relay, X.25, Signaling System 7 (SS7), ISDN D-channel signaling, and LAN/WAN data transport.
- Under minimal host supervision, the MUSYCC manages a linked list of channel data buffers in host memory by performing direct memory access (DMA) for the 128 channels, Tx and Rx.

The MUSYCC interfaces with four independent serial data streams, such as T1/E1/J1 signals, and then transfers data across the peripheral component interface (PCI) bus to system memory at a rate of 132 MBps. The OSS-wanPCI-CxT1E1 will operate for both T1 (1.544MHz) or E1 (2.048MHz). Logical channels can be mapped as any combination of DS0 time slots to support ISDN hyperchannels (Nx64Kbps) or as any number of bits in a DS0 for subchanneling applications (Nx8Kbps)

COMET framer

The four PMC Sierra Framer interface components (PM4351 COMETs) allow the software to select between T1 (100 Ohm), E1 (120 Ohm), and J1 configurations.

I/O

T1/E1/J1 ports

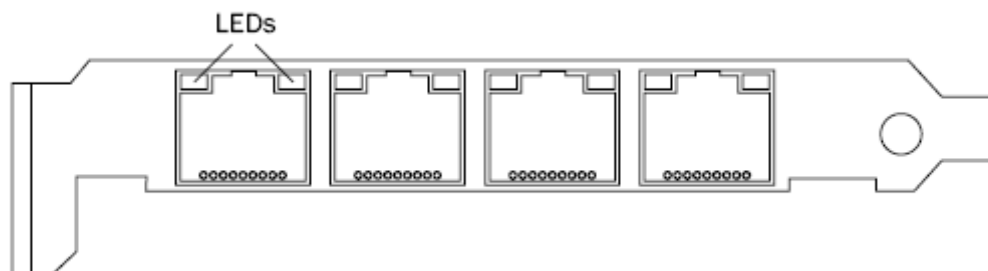
The OSS-wanPCI-CxT1E1 supports four T1/E1/J1 ports. Four onboard COMET chips provide the framer and LIU supporting the four T1/E1/J1 ports. The CSU components reside on the module. The tip and ring for each port are routed to fully shielded RJ48C connectors mounted behind the PMC bezel.

T1/E1/J1 and COMET register settings

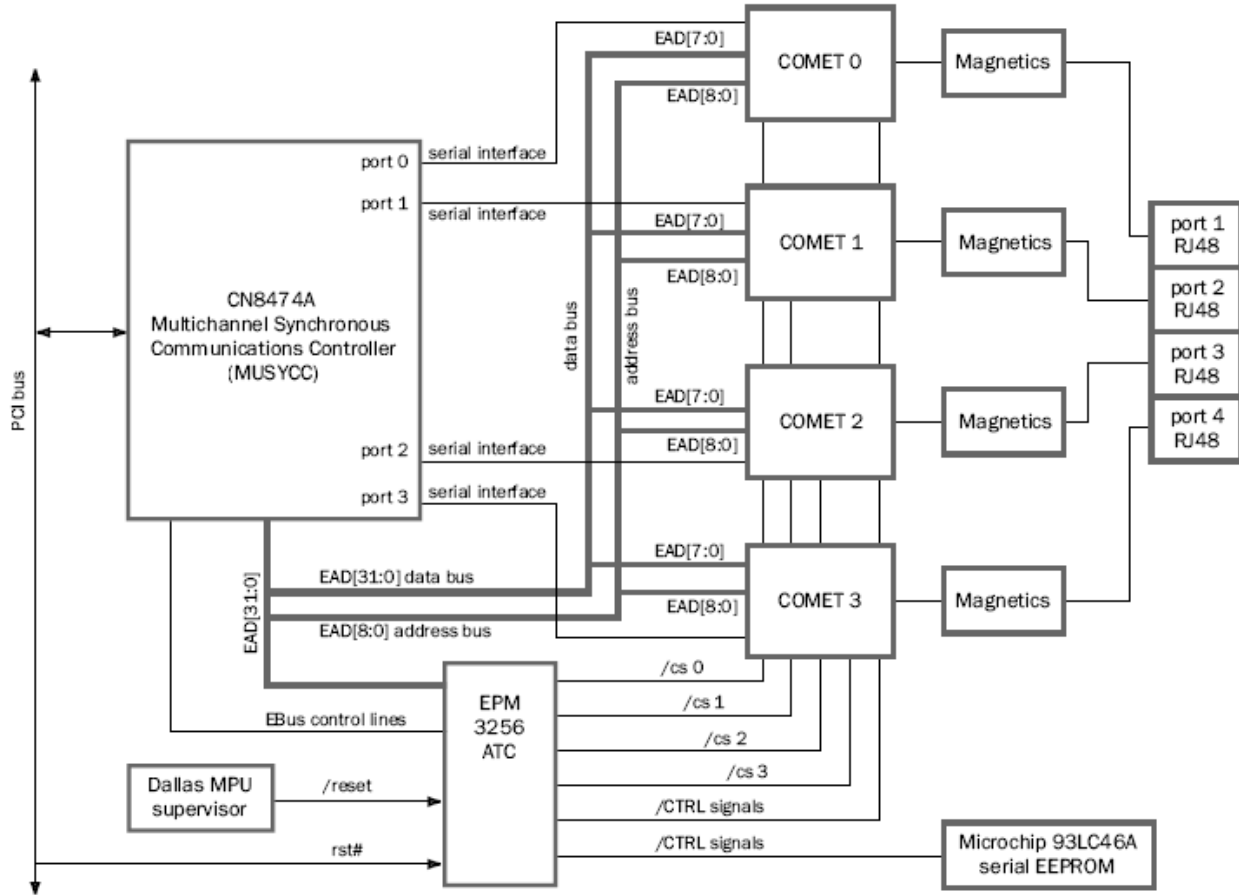
COMET register settings impact the T1/E1/J1 pulse waveform and therefore, your telecom (FCC part 68 and CEMark) approval. Register tables are available in the PM4351 COMET COMBINED T1/E1 TRANSCIEVER/FRAMER DATASHEET from PMC-Sierra (PMC-970624). See Chapter 6, In-System Programmable Logic Device (iSPLD), for information on the initialization of the waveform registers and equalizer registers.

Front Panel

The front panel will have 1, 2 or 4 RJ48 ports. The front panel for the OSS-wanPCI-C4T1E1 is shown below.



Block Diagram



Connectors

The OSS-wanPCI-CxT1E1 supports four T1/E1/J1 ports. Four PM4351 COMET chip sets provide the framer and LIU to support the four T1/E1/J1 ports. The CSU components reside on the OSS-wanPCI-CxT1E1. The tip and ring for each port are routed to the individual fully shielded RJ48C connector mounted to the PMC bezel.

Connectors (continued)

The pin-out for the PCI edge connector is show below

A	B	Pin		Pin	A	B
TRST#	-12V	1		2	+12V	TCK
TMS	GND	3		4	TDI	TDO
+5V	+5V	5		6	INTA#	+5V
INTC#	INTB#	7		8	+5V	INTD#
Reserved	PRSNT1#	9		10	VC(I/O)	Reserved
Reserved	PRSNT2#	11		12	Keyway	Keyway
Keyway	Keyway	13		14	Reserved	Reserved
RST#	GND	15		16	V(I/O)	CLK
GNT#	GND	17		18	GND	REQ#
Reserved	V (I/O)	19		20	AD[30]	AD[31]
+3.3V	AD[29]	21		22	AD[28]	GND
AD[26]	AD[27]	23		24	GND	AD[25]
AD[24]	+3.3V	25		26	IDSEL	C/BE[3]#
+3.3V	AD[23]	27		28	AD[22]	GND
AD[20]	AD[21]	29		30	GND	AD[19]
AD[18]	+3.3V	31		32	AD[16]	AD[17]
+3.3V	C/BE[2]#	33		34	FRAME#	GND
GND	IRDY#	35		36	TRDY#	+3.3V
GND	DEVSEL#	37		38	STOP#	GND
+3.3V	LOCK#	39		40	Reserved	PERR#
Reserved	+3.3V	41		42	GND	SERR#
PAR	+3.3V	43		44	AD[15]	C/BE[1]#
+3.3V	AD[14]	45		46	AD[13]	GND
AD[11]	AD[12]	47		48	GND	AD[10]
AD[09]	M66EN	49		50	GND	GND
Connector Key	Connector Key	51		52	C/BE[0]#	AD[08]
+3.3V	AD[07]	53		54	AD[06]	+3.3V
AD[04]	AD[05]	55		56	GND	AD[03]
AD[02]	GND	57		58	AD[00]	AD[01]
V (I/O)	V (I/O)	59		60	REQ64#	ACK64#
+5V	+5V	61		62	+5V	+5V

Memory Map

The Expansion Bus (EBus) that carries the data on the OSS-wanPCI-CxT1E1 is connected to six byte-wide devices. These devices are the four COMETs, the serial EEPROM, and the iSPLD. The EBus interface uses the lower 20 bits from the PCI address line (AD[19:0]) to construct a byte address for the EBus. Specifically, PCI address lines AD[19:2] are remapped to EBus address lines EAD[17:0].

Device	PCIAddress
COMET 1	xxx80000 Hex
COMET 2	xxx90000 Hex
COMET 3	xxxA0000 Hex
COMET 4	xxxB0000 Hex
SERIAL EEPROM	xxxC0000 Hex
iSPLD	xxxD0000 Hex

Only single D-word (32-bit) PCI operations can be performed when accessing the EBus. Please refer to the N8474/CN8474A specification for more detail. All EBus accesses are on the least significant byte of the PCI bus and are aligned on the 32-bit boundary.

Serial EEPROM

Board serial numbers are stored in a Microchip 93LC46A and packaged in a small outline integrated circuit. This device can hold 1024 bits organized in a 128x8 format. The PCI host reads and writes to this device in a bit serial fashion.

InstructionSB	SB	OP code	EEPROM address bits							Data IN	Data OUT	# CLK cycles
Erase	1	11	A6	A5	A4	A3	A2	A1	A0	--	RDY_/BSY	10
Erase All	1	0	1	0	X	X	X	X	X	--	RDY_/BSY	10
Disable Erase/Write	1	0	0	0	X	X	X	X	X	--	HIGH-Z	10
Enable Erase/Write	1	0	1	1	X	X	X	X	X	--	HIGH-Z	10
Read	1	10	A6	A5	A4	A3	A2	A1	A0	--	D7-D0	18
Write	1	1	A6	A5	A4	A3	A2	A1	A0	D7-D0	RDY_/BSY	18
Write All	1	0	0	1	X	X	X	X	X	D7-D0	RDY_/BSY	18

Extended address bit definitions

Data Bit	Description
0	Data Out
1	Data In
2	Chip Select

Note: Insert a 500ns delay between each bit/write operation

Enable EEPROM

1. Set the chip-select bit and write a one to the EEPROM (serial bit).
2. Keep the chip-select bit set and write the EWEN bit sequence. This includes the don't care address bits.
3. Write the last byte with both the chip-select and data-out bits at zero.

Disable EEPROM

1. Set the chip-select bit and write a one to the EEPROM (serial bit).
2. Keep the chip-select bit set and write the EWDS bit sequence. This includes the don't care address bits.
3. Write the last byte with both the chip-select and data-out bits at zero.

Writing to the EEPROM

1. Enable EEPROM.
2. Set the chip-select bit and write a one to the EEPROM.
3. Keep the chip-select bit set and write the WRITE bits in two writes to the EEPROM.
4. Keep the chip-select bit set and do seven writes indicating the address of interest.
5. Keep the chip-select bit set and do eight writes with the data byte to load. Start with the most significant bit, D7.
6. Write a byte with both the chip-select and data-out bits at zero.
7. Write a byte again with the chip-select bit set.
8. Do two reads of the EEPROM. Discard the first read and check the second read for the data-in bit to be at zero.
9. Periodically read the data-in bit until a one is found.
10. Write a byte with both the chip-select and data-out bits at zero.
11. Disable EEPROM.

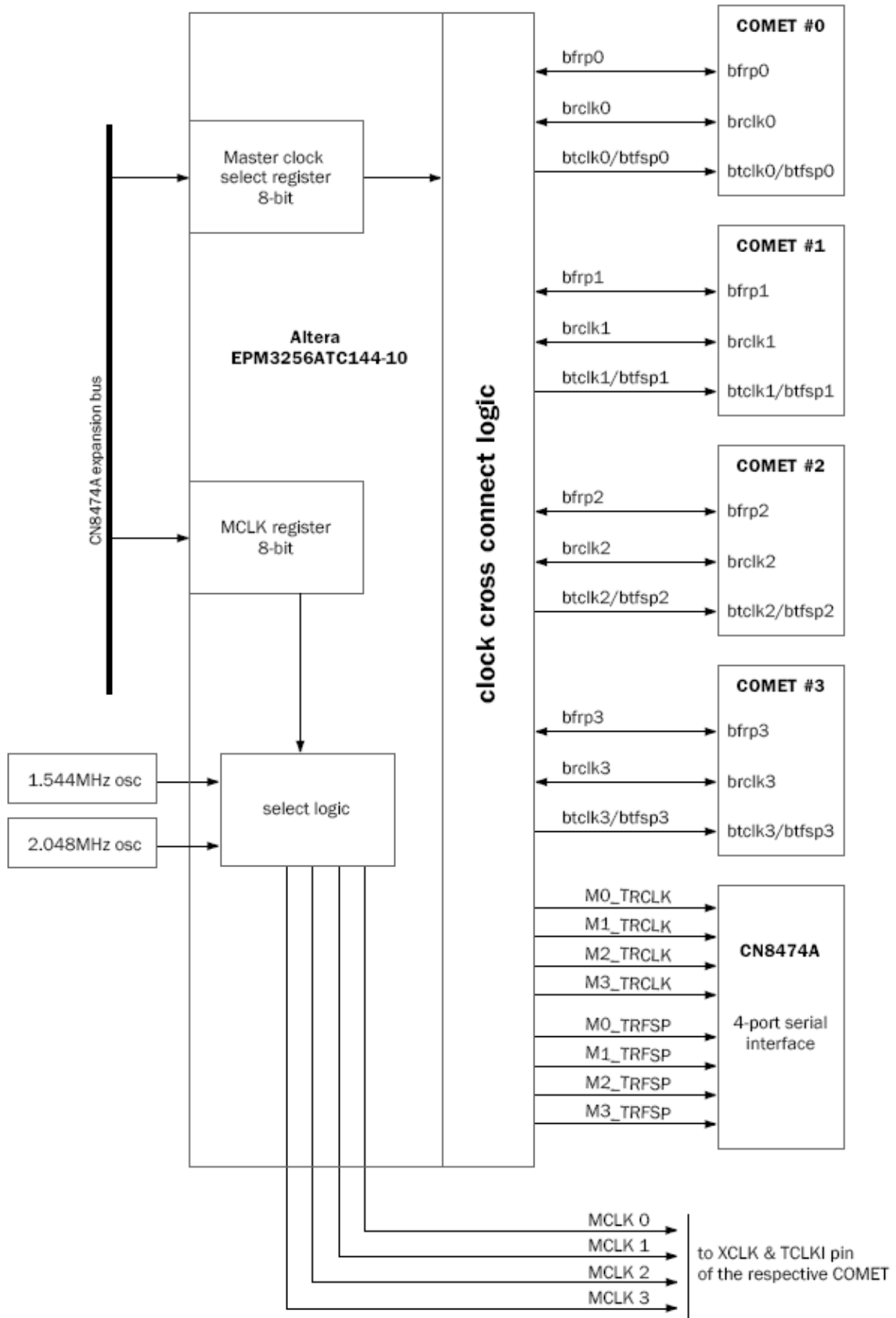
Reading from the EEPROM

1. Set the chip-select bit and write a one to the EEPROM.
2. Keep the chip-select bit set and write the READ bits in two writes to the EEPROM.
3. Keep the chip-select bit set and do seven writes indicating the address of interest.
4. Keep the chip-select bit set and do nine reads. Discard the first read. The eight remaining reads take the data from the data-in bit and shift it to the least significant bit position. Data is read starting from most significant bit position, D7. (Remember the data-in bit is at position one.)
5. Write a byte with both the chip-select and data-out bits at zero.

Clock/Frame Pulse Routing Matrix

Any one of the framers can provide the clock for data synchronization. The host, via the MCSR (Master Clock Select Register) can decide which framer provides the clock. After power-up or reset, the MCSR is reset and all framers synchronize to the clock input provide by XCLK. XCLK is an input to the framers and its source is one of the two on board oscillators (T1 or E1) and controlled by the MCLK register. Upon power up or reset, the MCLK register provides T1 clock to all framers. Thereafter, the host can manipulate the MCLK register to provide T1 or E1 to any framer. See diagram next page

Clock/Frame Pulse Routing Matrix (continued)



Initialization

The OSS-wanPCI-CxT1E1 must be reset and initialized before it can be programmed. This section contains the necessary code to reset and initialize the waveform and the equalizer registers.

Reset Functions

After powerup, a Dallas DS1817 chip generates a reset that forces all components on the OSS-wanPCI-CxT1E1 into a reset state that terminates after 150ms. A second reset source is the PMC's #RST pin from the PCI or VME host.

The host must configure the MUSYCC as a PCI master; this allows the MUSYCC to access host memory addresses. The host also must write to the function 1 PCI configuration command register, enabling access to the OSS-wanPMC-CxT1E1EBus space.

The following steps outline the sequence of events to bring up the board after a reset condition.

1. Map function 0 and function 1 into the PCI's memory address space. Each function requires at least 1 megabyte of memory space.
2. Enable memory accesses onto the PMC's space.
3. Write to the Global Configuration Descriptor in the MUSYCC that sets up the access time and enables the EBus for individual accesses.
4. Depending on how you want the board configured, write to the MCLK register next to configure which ports are E1 and which are T1. Then write to the master clock select register (MCSR) to define which port(s) should be master.
5. Initialize the COMETs based on the MCSR setting.
6. Initialize the MUSYCC to support your specific requirements.

COMET and MUSYCC Initialization

The COMETs and the MUSYCC must be initialized so that the data being clocked in and out of the MUSYCC occurs on the proper edges. The following settings serve both master and slave clock modes in the COMET. These lines of code initialize the clock edge to strobe data out of the MUSYCC, out of the COMET, and on the receive side as well.

COMET configuration for the powerup default settings of the MCLK and MCS registers as master

```
Register 0x30; BRIF Configuration
NXDSO[1-0] = 0
CMODE = 0      BRCLK as an output
```

```
DE = 0: Use the falling edge of BRCLK
FE = 0: Use falling edge of BRCLK
```

```
Register 0x31; BRIF Frame Pulse Configuration
FPMODE = 0      BRFP as an output
```

```
Register 0x40; BTIF Configuration
NXDSO[1,0] = 0
CMODE = 1      BTCLK as an input
```

```
DE = 1: Use the rising edge of BTCLK
FE = 1: Use rising edge of BTCLK
```

```
Register 0x41; BTIF Frame Pulse Configuration
FPMODE = 1      BTFP as an input
```

COMET configuration for the slave setting

Register 0x30; BRIF Configuration

NXDSO[1,0] = 0

CMODE = 1 BRCLK as an input

DE = 0: Use the falling edge of BRCLK

FE = 0: Use falling edge of BRCLK

Register 0x31; BRIF Frame Pulse configuration

FPMODE = 1 BRFP as an input

Register 0x40; BTIF configuration

NXDSO[1,0] = 0

CMODE = 1 BTCLK as an input

DE = 1: Use the rising edge of BTCLK

FE = 1: Use rising edge of BTCLK

Register 0x41; BTIF Frame Pulse Configuration

FPMODE = 1 BTFP as an input

Note: NXDSO[1,0] This is the recommended setting, full frame. For other configurations, we recommend configuring the MUSYCC for that specific mode of operation.

Serial EEPROM

A 500ns delay is necessary for both read and write cycles of the serial EEPROM. Since the MUSYCC's data cycle time is approximately 300ns, the algorithm by which data is read from the serial EEPROM in a timely fashion will be as follows:

- The EEPROM must go through an EEPROM enable command at least once and is not disabled until the operation is complete. Only PCI single writes and reads can be used.
- A minimum of 500ns delay must exist between each single host access to and from the serial EEPROM.

Global configuration descriptor

BLAPSE[2-0] = 7

ECKEN = 1 Enable PCI clock to the EBUS

MPUSEL = 0

ALAPSE[1-0] = 3

ELAPSE[2-0] = 7

PORTMAP[1-0] = 0

Port configuration descriptor

ROOF_EDGE = 0 It is not used on this product

RSYNC_EDGE = 1 Rising edge

RDAT_EDGE = 1 Rising edge

TSYNC_EDGE = 1 Rising edge

TDAT_EDGE = 0 Falling edge

In-System Programmable Logic Device (iSPLD)

The In-System Programmable Logic Device (iSPLD) contains all of the necessary logic required by the CN8474A to communicate with its peripheral components. The iSPLD serves two purposes:

1. As a general logic device, supplying correct signal timing and address decoding for chip selects to the COMETs and EEPROM.
2. To provide registers to control the crystal routing and BRCLK routes to and from the COMETs and MUSYCC.

The iSPLD is an Altera EPM3256AE and serves the following logic functions:

- T1/E1/J1 clock routing to all COMETs
- COMET interrupts
- Serial EEPROM control
- COMET control
- LED control
- Master clock connections
- Reset functions

iSPLD registers, base address (EAD) = 0xD0000

Address offset	Register type	Function
0x0	Write/read	MCSR
0x4	Write/read	MCLK register
0x8	Write/read	LED register
0xC	Read only	Interrupt register

iSPLD Control

Write/read operations executed by the CN8474A via its EBus are translated to the appropriate timing for the PMC4351. The iSPLD decodes the address and generates the chip-select levels for each of the COMETs

Master Clock Select Register

Any or all of the COMETs can provide the clock for data synchronization. The host, via the MCSR, decides which COMET provides the clock. At reset, each COMET provides the clock for its port and must be configured as the master. In modes other than default or reset, one port is assigned the master with the iSPLD routing this clock to the remaining COMETs and MUSYCC.

The MCSR in the iSPLD can be written to and read by the PCI host. Immediately after powerup or host reset this register is initialized to all zeros. By default, COMET 1 serves to provide the master clock. The host may then select the clocking needs via the MCSR. See Master Clock Registers Table on next page for information about the MCSR and clocking information.

The MCSR in the CPLD is a read/write register combined with the Board ID Register (BIDR), a read-only register. The power-up default value of this register is 10 Hex.

BIDR Register – Address = 0xD0000				MCSR Register – Address = 0xD0000			
Read Only				Read/Write			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	1	MCSR3	MCSR2	MCSR1	MCSR0

Master Clock Registers (MCSR)

MCSR	Clock Source
00 Hex	All ports (COMETs) use their individual backplane clock as the clocksource used by their respective MUSYCC ports. NOTE: All COMETs must be initialized in master mode. COMET 1 provides clocking to MUSYCC port 0. COMET 2 provides clocking to MUSYCC port 1. COMET 3 provides clocking to MUSYCC port 2. COMET 4 provides clocking to MUSYCC port 3.
01 Hex	Port 1 (COMET 1) uses its backplane clock to provide the source clocking for all other COMETs including the MUSYCC ports. NOTE: COMET 1 must be initialized in master mode. COMETs 2, 3, and 4 must be initialized in slave mode.
02 Hex	Port 2 (COMET 2) uses its backplane clock to provide the source clocking for all other COMETs including the MUSYCC ports. NOTE: COMET 2 must be initialized in master mode. COMETs 1, 3, and 4 must be initialized in slave mode.
03 Hex	Port 3 (COMET 3) uses its backplane clock to provide the source clocking for all other COMETs including the MUSYCC ports. NOTE: COMET 3 must be initialized in master mode. COMETs 1, 2, and 4 must be initialized in slave mode.
04 Hex	Port 4 (COMET 4) uses its backplane clock to provide the source clocking for all other COMETs including the MUSYCC ports. NOTE: COMET 4 must be initialized in master mode. COMETs 1, 2, and 3 must be initialized in slave mode.

Note: The backplane clock is the clock between the COMET and the MUSYCC.

The COMET decides if the backplane clock is sourced by the central office or the onboard oscillator

Master Clock register and Board Type Register

The framers require a MCLK that can be either T1 (1.544MHz) or E1 (2.048MHz). Two onboard oscillators are provided to be the source of those clocks. The MCLK register is used to select between the two oscillators. The MCLK register is a write/read register set to default to zero after powerup or system reset. The MCLK Register is a read/write register combined with the Board Type Register (BTYP), a read-only register. The power-up default value of this combined register is X0 Hex, where X depends on the number of ports available on the board. Each COMET requires an MCLK that can be either T1 (1.544 MHz) or E1 (2.048 MHz). Two on-board oscillators are provided to be the source of those clocks. The MCLK Register is used to select between the two oscillators for each port.

BTYP Register – Address = 0xD0001				MCLK Register – Address = 0xD0001			
Read Only				Read/Write			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Type 1	Type 0	Port 3	Port 3	Port 1	Port 0

Port0 = 0 COMET 0 MCLK = T1

Port 0= 1 COMET 0 MCLK = E1

Port1 = 0 COMET 1 MCLK = T1

Port 1= 1 COMET 1 MCLK = E1

Port2 = 0 COMET 2 MCLK = T1

Port2= 1 COMET 2 MCLK = E1

Port3 = 0 COMET 3 MCLK = T1

Port 3= 1 COMET 3 MCLK = E1

Type[1:0] = 00 4 Ports Available

= 01 1 Ports Available

= 10 2 Ports Available

Other values are reserved for future products. Bits 7 and 8 are Reserved bits

LED register

There are ten LEDs mounted on the front panel connectors. Eight LEDs are programmable and can be used for AIS and RAI alarms. The ninth LED is the power LED (see Section 6-2). The tenth LED is the power LED. The table below defines each bit in the LED register

LED Register – 0xD0002 Read/Write							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CR8 Yellow	CR9 Green	CR6 Yellow	CR7 Green	CR4 Yellow	CR5 Green	CR2 Yellow	CR3 Green

0 = OFF

1 = ON

Interrupts

The MUSYCC requires the use of PCI signals INTA# and INTB#.

- INTA# is driven by the MUSYCC to indicate a MUSYCC layer-2 interrupt condition to the PCI host processor.
- INTB# is driven by the MUSYCC to notify the PCI host processor of an interrupt pending from the EBus. Interrupts from the COMETs are latched in a register resident in the iSPLD. The interrupts from the COMETs are logically OR-ed to generate an interrupt to the MUSYCC. The MUSYCC transfers this interrupt from the EBus to the PCI INTB# pin when enabled in the Global Configuration Descriptor. The PCI host processor reads the interrupt register to determine which device was responsible for the interrupt. These bits are direct links from each COMET. They are cleared only when that COMET.s interrupts have been cleared

Interrupt Register – Address Offset = 3 – Read Only							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	COMET 4	COMET 3	COMET 2	COMET 1

0 = No interrupt

1 = Interrupt pending

X = Reserved (don.t care)

The appropriate COMET clears the interrupt bit when the interrupt is serviced

Power LED

The ninth LED is the power LED. This bicolor LED indicates the status of the 2.5V regulator. The power LED is not software accessible.

Power LED Bicolor	2.5 Volt Status
Green	Power is OK
Red	Power is BAD

Reset LED

The reset LED is a yellow LED located on the primary side of the board near the top edge. The LED is on when the Board Reset signal is active. The Board Reset signal is connected to the CN8474 and the four COMETs, and is the logical OR of the PCI Reset signal with the status signals from both of the reset devices.

JTAG

The JTAG chain supports the following mutually exclusive functions: JTAG and CPLD programming. During CPLD programming, the chain is connected such that the devices other than the CPLD are excluded. During normal JTAG testing, all JTAG devices are included in the chain.

The wanADAPT-CxT1E1 has six (6) components that are capable of JTAG functionality. EPM3256 CPLD, CN8474 and the four COMETs capable of JTAG are connected in a chain. The board JTAG chain is not supported at the PCI connection. The following is the JTAG chain order:

JTAG	EPM3256A	CN8474A6	Comet #3	Comet #2	Comet #1	Comet #0
	#1	#2	#3	#4	#5	#6

For

2-port and 1-port options, on-board 0-ohm resistors are used to bypass the appropriate COMETs.

Note: Framer TDO signals will require 10K pull up resistors

JTAG TAP Pin Assignments

A standard JTAG Test Access Port (TAP) connector is used with the following pin assignments:

JTAG TAP Connector Pin Assignments	Pin #	Pin #	JTAG TAP Connector Pin Assignments
/TRST	1	2	GND
TDI	3	4	GND
TDO	5	6	GND
TMS	7	8	GND
TCK	9	10	GND

ByteBlaster Pin Assignments

The table below is the Altera ByteBlasterMV connector's pin assignments: The ByteBlaster plugs into a standard 10-pin shrouded header. The key (i.e., notch) should be oriented on the side with the configuration or programming signals, not on the side with VCC and GND.

ByteBlaster Connector Pin Assignments	Pin #	Pin #	ByteBlaster Connector Pin Assignments
TCK	1	2	GND
TDO	3	4	VCC
TMS	5	6	NC
NC	7	8	NC
TDI	9	10	GND