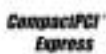


Single Port Channelized T3PMC

OSS-wanPMC-C1T3



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Description

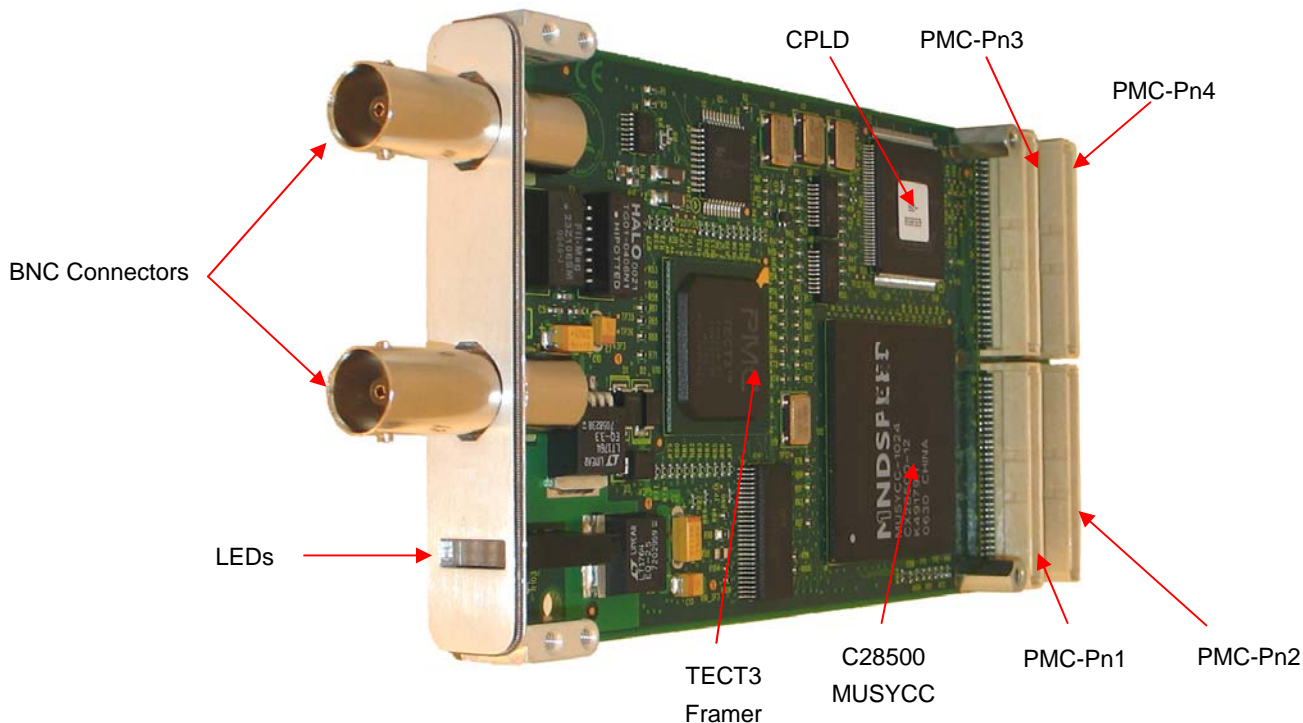
The OSS-wanPMC-C1T3 is a PMC module that incorporates a fully channelized T3 port with an HDLC transparent controller and a PMC interface. **There is no SS7 Support.** Transparent mode is possible at the DS0 level only. The card is software selectable between T1 and E1 over the T3 interface.

This product uses the Conexant CX28500 Multichannel Synchronous Communications Controller (MSCC) as the PCI interface and HDLC controller. Its function is to provide the PCI Bus interface, control the local Expansion Bus (EBUS) for board/transparent data to its own conventional TDM ports.

The PCI interface conforms to the PCI 2.1 specification. It transfers 64 bits of data at up to 66MHz. 3.3V and 5V PCI bus signaling is supported. DMA transfers to and from host memory are also supported.

PMC Sierra's TECT3 (PM4328) is used to translate data between the MSCC's conventional TDM lines and the DS3 LIU. This includes 28 T1 / 21 E1 framers, an M13 mux and a DS3 framer. Exar's XRT73L00A Line Interface Unit (LIU) provides signal conditioning and various loopback capabilities.

An IDT82V3001A WAN PLL provides clock and frame synchronization for the system side TDM ports.



Initial Set-Up

Unpacking Instructions

1. If the carton is damaged when you receive it, request that the carrier's agent be present when you unpack and inspect the equipment.
2. After unpacking, verify that all items listed in the packing list are present.
3. Inspect the equipment for shipping damage.
4. Save all packing material for storage or return shipment of the equipment.
5. For repairs or replacement of equipment damaged during shipment, contact One Stop Systems, Inc. to obtain a Return Materials Authorization (RMA) number and further shipping instructions.

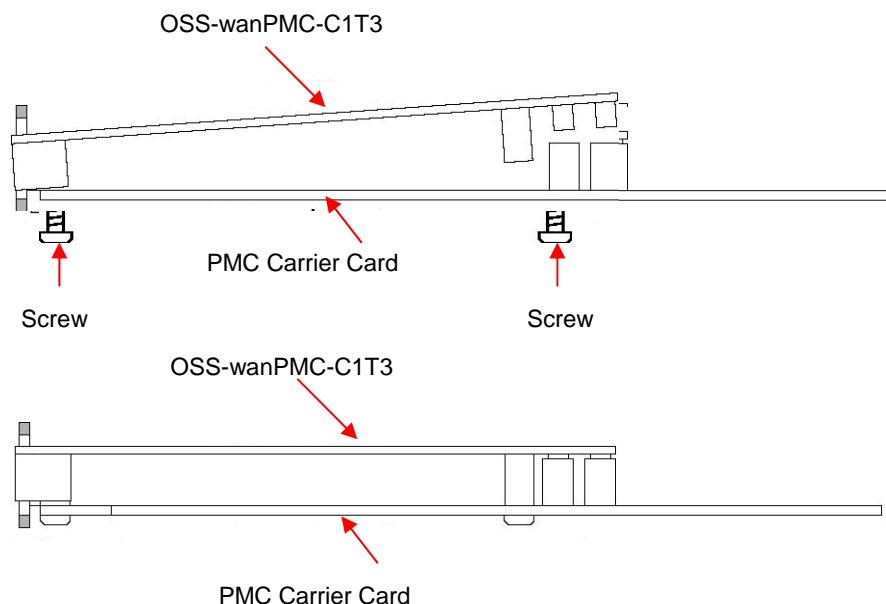
Installation and Removal

1. Power down the host system.
2. Open the chassis according to your system documentation.
3. Let the power supply cool down, if necessary.
4. Remove the host board from the system.
5. Remove the OSS-OSS-wanPMC-C1T3 from the protective bag, observing proper ESD safety procedures.

Installing the OSS-wanPMC-C1T3:

1. Press the OSS-wanPMC-C1T3 bezel into the cutout in the PMC carrier I/O panel. The gasket around the OSS-OSS-wanPMC-C1T3 bezel makes a tight fit to ensure an electromagnetic seal. Check that the bezel and gasket are pressed firmly into the carrier I/O.
2. Press the OSS-wanPMC-C1T3 down onto the carrier so PN1–PN4 plug into JN1–JN4 on the PMC carrier.
3. Install four screws to secure the in place

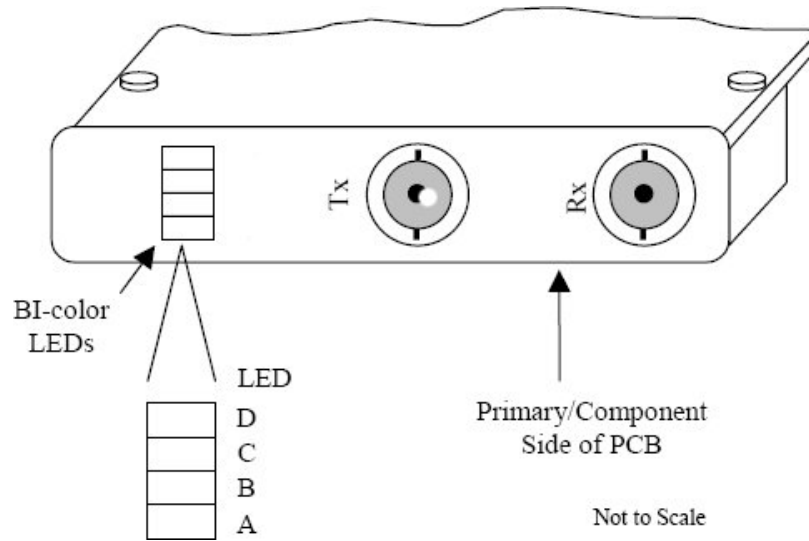
Installation Diagram



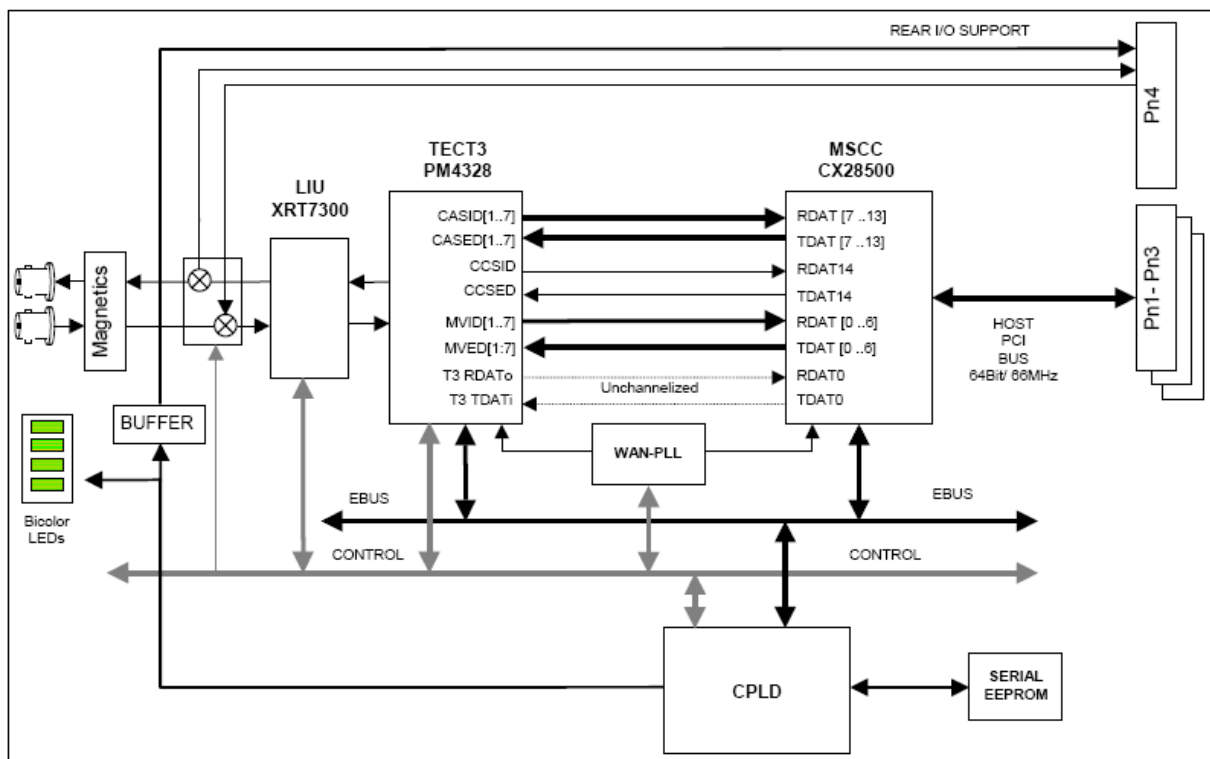
Specifications

Electrical/Mechanical Specifications	
Form Factor:	PCI Mezzanine Card (PMC) [5V or 3.3V]
Dimensions (H x L):	5.86 x 2.91 inches (148.8 x 73.9mm)
Front Panel Connectors:	Two BNC Connectors
Front Panel Indicators:	Four Bi-color LEDs
Power Consumption (designed to meet the following conditions)	
	7.5W maximum @ 3.3V
Operating Environment (designed to meet the following conditions)	
Temperature Range:	-5° to 55°C (23° to 136°F)
Relative Humidity:	20 to 80% non-condensing
Shock:	30g acceleration peak (11ms pulse)
Vibration:	5-17 Hz 0.5" double amplitude displacement; 7-2000Hz, 1.5g acceleration.
Agency Compliance Designed to meet, but not tested	
	NEBS, UL 60950, FCC ClassA, CE Mark, VCCI
MTBF (Telecordia TR-332 Version 6)	
	395,000 hours

Front Panel



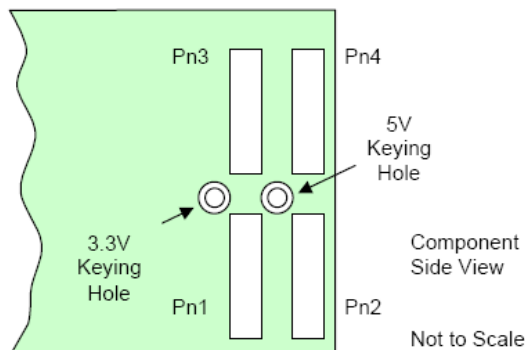
Block Diagram



Keying

The OSS-wanPMC-C1T3 can be operated in a 5V or 3.3V signaling environment. The signaling environment is determined by the voltage on the PCI VIO pins and is host-specific.

When installing the card on a host, the voltage coding key must be installed in accordance with the host requirements. If the Host is capable of accommodating both 3.3 and 5 volt signaling, then the 3.3 volt signaling is preferred



Power

Power is supplied to the OSS-wanPMC-C1T3 by the carrier board. Current is drawn from the 5V and 3.3V power pins. The tolerance on the 5V and 3.3V supply is $\pm 10\%$ in accordance with the PCI Local Bus Specification

PCI Bus Interface

The OSS-wanPMC-C1T3 interfaces to the host system using a 32/64bit/33/66MHz PCI 2.1 compliant PCI bus controller built into the Conexant CX28500 (MSCC). MSCC also includes a 32-bit expansion port (EBUS) for bridging the PCI bus to local peripherals.

Following are the specifications of OSS-wanPMC-C1T3's PCI interface:

- PCI Local Bus Specification Revision 2.1 compliant.
- 32/64 bit, 33/66 MHz PCI is supported (see note Section 3.1.1).
- PCI master and slave capable.
- Responds only to Function 0 (access to all HDLC processing and EBUS service requests) cycles.
- EBUS (peripheral control) access via service requests using configurable memory mapping features.
- Fast Back to Back DMA transactions, Master and Target.
- Implements universal signaling (3.3 V I/O and 5V tolerant) by wiring MSCC's Vgg pin to PCI VIO pin.
- INTA# supported only. INTA# indicates a MSCC layer 2 interrupt condition. Note: INTB# is wired direct from the CPLD and indicates a TECT3, LIU or WAN PLL interrupt pending.
- Subsystem Vendor ID field in PCI configuration space is not supported by MSCC.
- The JTAG test port is supported and implemented through the standard JTAG pins defined in the PMC standard.
- PCI Reset immediately tri-states the MSCC PCI interface and the EBUS interface. After reset is removed the PCI configuration space Function 0 must be reinitialized.
- The BUSMODE pins are configured to indicate a PCI compliant assembly. S-Bus is not supported.

Busmode Pins

Since OSS-wanPMC-C1T3 supports only the PCI bus protocol at the PMC connectors, the BUSMODE1# pin is asserted LOW for two reasons only; (1) to indicate its presence to the host, and (2) to indicate that it is capable of performing PCI Bus protocol (see table below). The OSS-wanPMC-C1T3 responds within ten PCI clock cycles after detecting the state of BUSMODE[4:2]# pins.

BUSMODE[4:2]# state (input)	Mode	BUSMODE1# output state	Response explanation
000	“Card Present” test.	0	“Card Present” mode. No bus protocol is used and card is held in reset
001	Return Card Present if PCI capable and uses PCI protocol.	0	Capable of performing PCI protocol.
All other states	-	1	Card held in reset.

EBUSConfiguration

To access devices on EBUS, MSCC’s EBUS Configuration Descriptor (offset 0x08114) must be set as follows:

Bit Field	Name	Value	Description
31:14:00	RSVD	0	Reserved
13	ECLKDIV(1)	Per Bus Speed	EBUS Clock divide (see note below)
12	MPUSEL	0	Expansion bus Motorola style
11	ECKEN	1	Enable EBUS Clock
10:08	ALAPSE[2:0]	0	Extend address phase 0 +1 ECLK periods
7:04	BLAPSE[3:0]	0	No bus access wait between cycles
ELAPSE[3:0]	7	Extend data phase 7 +1 ECLK periods	

⁽¹⁾ **Note** : CX28500 supports 66MHz operation. M66EN signal is utilized for this purpose. The local EBUS clock may operate at same clock rate or ½ the clock rate as the PCI Bus. Setting the ECLKDIV bit in the EBUS Configuration Register to “1” (Default) will divide the EBUS clock to ½ the PCI clock rate. The EBUS must always operate at 33MHz for correct peripheral control timing. In a 66Mhz PCI system the ECLKDIV default value will suffice. In a 33Mhz PCI system, the ECLKDIV bit should be changed to a zero. A bit in the CPLD has been provided to indicate the state of the M66EN pin. If the M66EN bit in the CPLD’s General Purpose Register (GPR) is a zero (33Mhz PCI), software should change the ECLKDIV bit to a zero. The EBUS will then operate at 33MHz instead of 16.666MHz.

To change the ECLKDIV bit, the clock must first be disabled with the ECKEN bit and then re-enabled.

EBUS Service Request Mechanism

Once configured and enabled, the Host can configure local devices connected to the EBUS by issuing the EBUS Access Service Request (EBUS_WR or EBUS_RD). The Service Request Mechanism uses shared memory locations that must be initialized prior to service request processing. The command is a three dword memory location with the following dword fields. Access Control Field, Shared Memory Pointer and the EBUS Base Address Offset

Memory Map

MSCC allows access to a 31 bit Address memory range on its EBUS. The EBUS base address offset is a D-Word (32-bits) where the MSB (bit 31) must be set to 1 for all transactions. The OSS-wanPMC-C1T3 EBUS is connected to an 8-bit CPLD for on board registers and EEPROM control and the 8 bit TECT3 device. These devices connect so they occupy the lower order bits (bits [7:0]) of the EBUS. Bits [31:8] are not used for data transfer and are pulled high using pull-up resistors.

Dword Number	Bit 31					Bit 0
Dword 0	OPCODE	SACKIEN	Reserved	FIFO_Burst	EBUS Byte Enable	LENGTH
Dword 1	Shared Memory Pointer [0:32]					
Dword 2	EBUS Base Address Offset					
Dword 3	Reserved - set to all 1's					

HDLC Packet Processor

The HDLC controller is implemented in the Conexant CX28500 Multichannel Synchronous Communications Controller (MSCC). It can format and de-format up to 1024 logical HDLC channels that can span across multiple time slots or within sub-rates. The data is then transferred across the PCI Bus into system memory or sent out the TDM serial ports. **The part does not support SS7.**

The CN28500 should be configured to operate in conventional (TDM) mode. Modes are configured by programming the

Bit	Field Name	Value	Description
31:14:00	RSVD	0	Reserved
13	RXENBL	0	Receive Port Disabled –resets serial port
	1	Receive Port Enabled	
12	RSVD	0	Reserved
11:09	RPORT_TYPE	0	Unchannelized mode
		5	Nx64

RPORT_TYPE and **TPORT_TYPE** bit fields in the *RSIU Port Configuration Register* and the *TSIU Port Configuration Registers* respectively.

TSIU and RSIU Port Configuration Register

Device	EBUS Address Range
Reserved	0x00000-0x27FFF
TECT3	0x28000-0x2BFFF
Reserved	0x2C000-0x2FFFF
Serial EEPROM	0x30000-0x33FFF
CPLD	0x34000-0x37FFF
Reserved	0x38000-0x3FFFF

For Channelized operation, Ports 0 through 14 operate at 8.192 Mbps, 128 - 8 bit time slots per frame (i.e., 4xE1 rate). Frame synchronization pulses occur at 8KHz and are generated using Frame pulse outputs of IDT82V3001A (WAN PLL). Port 0 is capable of being used for Unchannelized T3 that operates at 44.210 Mbps (payload). This card has only one T3 interface so it will operate using either Port 0 in Unchannelized mode or Ports 0-14 at 4xE1 TDM mode but not both at the same time. For Unchannelized T3 set RPORT_TYPE and TPORT_TYPE = 0 for port 0 . For 4x E1 mode set RPORT_TYPE and TPORT_TYPE = 5 for ports 0-14 and the Time Slot map must have 128 time slots allocated to each port. The allocation is configured in the Time Slot Pointer Assignment Register. See Sections 6.6.6 and 6.7.6 in the CX28500datasheet.

Line Interface

The DS3 line interface is implemented using EXAR XRT73L00AIV. This device operates at 3.3V. The XRT73L00 is setup to operate in "Hardware Mode" not "Host Mode." Default settings of the device are such that it is fully operational at power-up. Software can configure the device for particular application via registers in the CPLD.

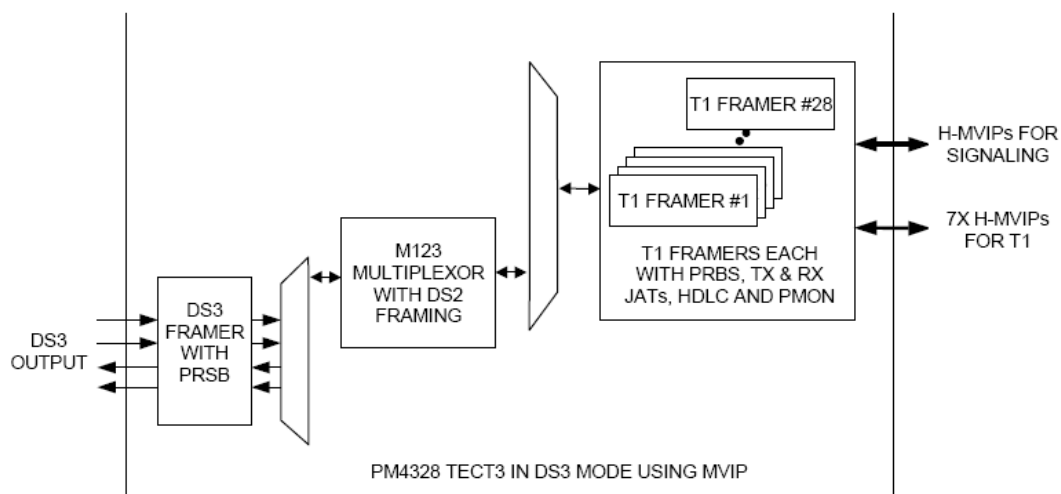
Note: Though the LIU can perform B3ZS encoding and decoding, this function is disabled on the OSS-wanPMC-C1T3. The TECT3 provides this feature and having control in two places can be a cause of potential confusion and problem. Since there is no loss of functionality and it minimizes the confusion as to where the encoding/decoding is done, what rail format is used (DR or SR) and how it is controlled, on the OSS-wanPMC-C1T3 pins 21 and 22 are tied together and pulled-high by the CPLD. This indicates that the encoder and decoder are disabled and DR data is used.

The LIU provides three sources of interrupts; no transmitter output (DMO), receiver loss of lock, and receiver loss of signal. These interrupts are enabled/disabled using the Interrupt Enable Register.. Refer to the XRT7300 data sheet for detailed description of these signals and for description of other features of the LIU.

Two 75 ohm BNC connectors are utilized to provide physical interface to the line. The signals to and from the connectors are transformer isolated. Both transmit and receive transformers are in the same module. A common mode is also provided and provision is made for access via a Rear Transition Module.

DS3 Framer and Multiplexer

The DS3 to TDM framing and multiplexing is accomplished using the PMC-Sierra PM4328 TECT3. This device integrates a DS3 framer, an M13 multiplexer, and 28 T1 (or 21 E1 framers) into a 324-ball PBGA package. Setup and configuration is accomplished via the local EBUS connected to the TECT3's 8-bit microprocessor interface

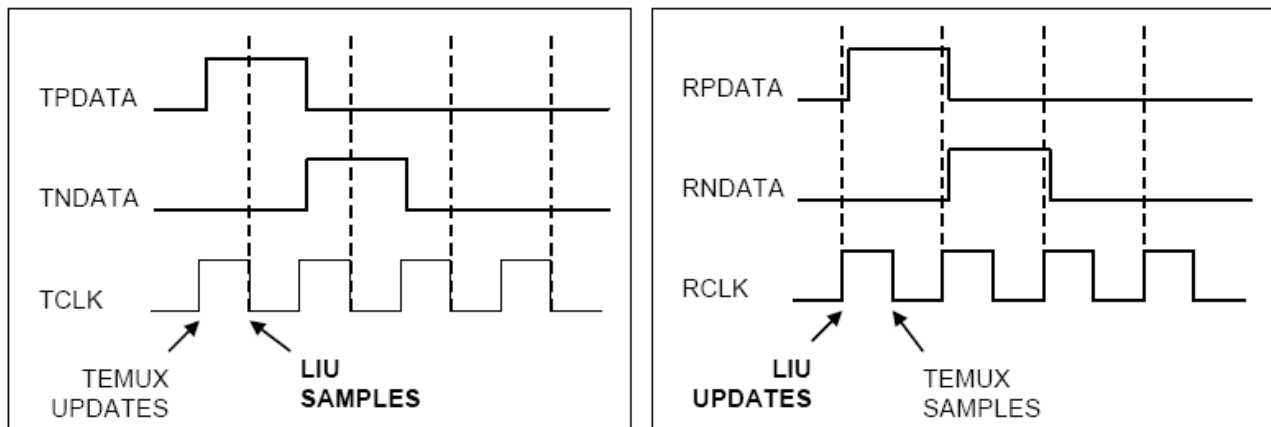


Clock	OSS-wanPMC-C1T3 Name	Frequency	Accuracy	Duty Cycle
TICLK	T3_CLK	44.736 MHz	20 ppm	40-60%
XCLK (**)	XCLK	37.056 MHz for T1 49.152 MHz for E1	32 ppm	50%
CTCLK (*)	CTCLK	1.544 MHz	32 ppm	40-60%
CMV8MCLK	MVCLK	16.384 MHz	32ppm	40-60%
CMVFPC	FRMCLK	4.096 MHz	32ppm	40-60%
Must be aligned with the falling edge of CMV8MCLK with no more than +/- 10ns skew.				

*CTLK is connected to the C1.5 -1.544MHz output of the WAN PLL. There is a zero ohm jumper that can change the connection of CTCLK to the C2o-2.048MHz output of the WAN PLL if needed

** The E1 mode requires a different XCLK frequency and, thus, a different oscillator. T1/E1 mode is software selectable

In hardware mode the LIU samples the transmit data on falling edge of the transmit clock and updates the received data on rising edge of the receive clock. Hence, the TECT3 must be configured to output the transmit data on rising edge of transmit clock and sample receive data on falling edge of receive clock. Figure 6 illustrates this data timing requirement between the LIU and the TECT3. The vertical lines in the figure below are from the point of view of the LIU. Note that the default state of TECT3 is opposite to that required and the TRISE and RFALL bits in the DS3 Master Transmit Line Options register must be set to get correct timing.



CIFP	CIFP	125 us	ramers.Used to align the ingress data to the system frame alignment.
CMVFPB	FRAME	125 us	Active Low pulse for 8.192Mbps H-MVIP. (See TECT3 Register at 0x0006)

IDT82V3001A WAN PLL

The IDT82V3001A WAN PLL provides clock and frame synchronization for the system side TDM ports. The full device part number is IDT82V3001A-PV in a 56 pin, TSSOP package.

The WAN PLL contains a Digital Phase Lock Loop (DPLL) that generates clocks and framing signals that are phase locked to a single reference input of either 2.048MHz, 1.544MHz or 8 KHz. The WAN PLL has three modes Normal, Holdover or Freerun. The modes are selected by setting PLL_M[0:1]bits in CPLD's PLL Control Register. The input frequency must be set by setting FSEL[0:1] bits in the CPLD's PLL Control Register. Default settings are Normal mode and input frequency reference = 1.544MHz. There are four outputs that can be monitored by reading Board Status Register in the CPLD. The first is LOCK which is set when the DPLL is frequency is locked with the reference. The other three outputs indicate the operating mode: Normal, Freerun or Holdover.

Connectors

Communication on the host PCI bus is done across three PMC connectors, **Pn1, Pn2, and Pn3**.

Pn1 32-bit PCI				Pn2 32-bit PCI				Pn3 64-bit PCI			
Pin #	Name	Name	Pin #	Pin #	Name	Name	Pin #	Pin #	Name	Name	Pin #
1	TCK	-12V	2	1	+12V	TRST#	2	1	PCI-RSVD	Ground	2
3	Ground	INTA#	4	3	TMS	TDO	4	3	Ground	C/BE[7]#	4
5	INTB#	INTC#	6	5	TDI	Ground	6	5	C/BE[6]#	C/BE[5]#	6
7	BUSMODE1#	+5V	8	7	Ground	PCI-RSVD	8	7	C/BE[4]#	Ground	8
9	INTD#	PCI-RSVD	10	9	PCI-RSVD	PCI-RSVD	10	9	V(I/O)	PAR64	10
11	Ground	3.3Vaux	12	11	BUSMODE2#	+3.3V	12	11	AD[63]	AD[62]	12
13	CLK	Ground	14	13	RST#	BUSMODE3#	14	13	AD[61]	Ground	14
15	Ground	GNT#	16	15	+3.3V	BUSMODE4#	16	15	Ground	AD[60]	16
17	REQ#	+5V	18	17	PME#	Ground	18	17	AD[59]	AD[58]	18
19	V(I/O)	AD[31]	20	19	AD[30]	AD[29]	20	19	AD[57]	Ground	20
21	AD[28]	AD[27]	22	21	Ground	AD[26]	22	21	V(I/O)	AD[56]	22
23	AD[25]	Ground	24	23	AD[24]	+3.3V	24	23	AD[55]	AD[56]	24
25	Ground	C/BE[3]#	26	25	IDSEL	AD[23]	26	25	AD[53]	Ground	26
27	AD[22]	AD[21]	28	27	+3.3V	AD[20]	28	27	Ground	AD[52]	28
29	AD[19]	+5V	30	29	AD[18]	Ground	30	29	AD[51]	AD[50]	30
31	V(I/O)	AD[17]	32	31	AD[16]	C/BE[2]#	32	31	AD[49]	Ground	32
33	FRAME#	Ground	34	33	Ground	PMC-RSVD	34	33	Ground	AD[48]	34
35	Ground	IRDY#	36	35	TRDY#	+3.3V	36	35	AD[47]	AD[46]	36
37	DEVSEL#	+5V	38	37	Ground	STOP#	38	37	AD[45]	Ground	38
39	Ground	LOCK#	40	39	PERR#	Ground	40	39	V(I/O)	AD[44]	40
41	PCI-RSDV*	PCI-RSVD	42	41	+3.3V	SERR#	42	41	AD[43]	AD[42]	42
43	PAR	Ground	44	43	C/BE[1]#	Ground	44	43	AD[41]	Ground	44
45	V(I/O)	AD[15]	46	45	AD[14]	AD[13]	46	45	Ground	AD[40]	46
47	AD[12]	AD[11]	48	47	M66EN	AD[10]	48	47	AD[39]	AD[38]	48
49	AD[09]	+5V	50	49	AD[08]	+3.3V	50	49	AD[37]	Ground	50
51	Ground	C/BE[0]#	52	51	AD[07]	PMC-RSVD	52	51	Ground	AD[36]	52
53	AD[06]	AD[05]	54	53	+3.3V	PMC-RSVD	54	53	AD[35]	AD[34]	54
55	AD[04]	Ground	56	55	PMC-RSVD	Ground	56	55	AD[33]	Ground	56
57	V(I/O)	AD[03]	58	57	PMC-RSVD	PMC-RSVD	58	57	V(I/O)	AD[32]	58
59	AD[02]	AD[01]	60	59	Ground	PMC-RSVD	60	59	PCI-RSVD	PCI-RSVD	60
61	AD[00]	+5V	62	61	ACK64#	+3.3V	62	61	PCI-RSVD	Ground	62
63	Ground	REQ64#	64	63	Ground	PMC-RSVD	64	63	Ground	PCI-RSVD	64