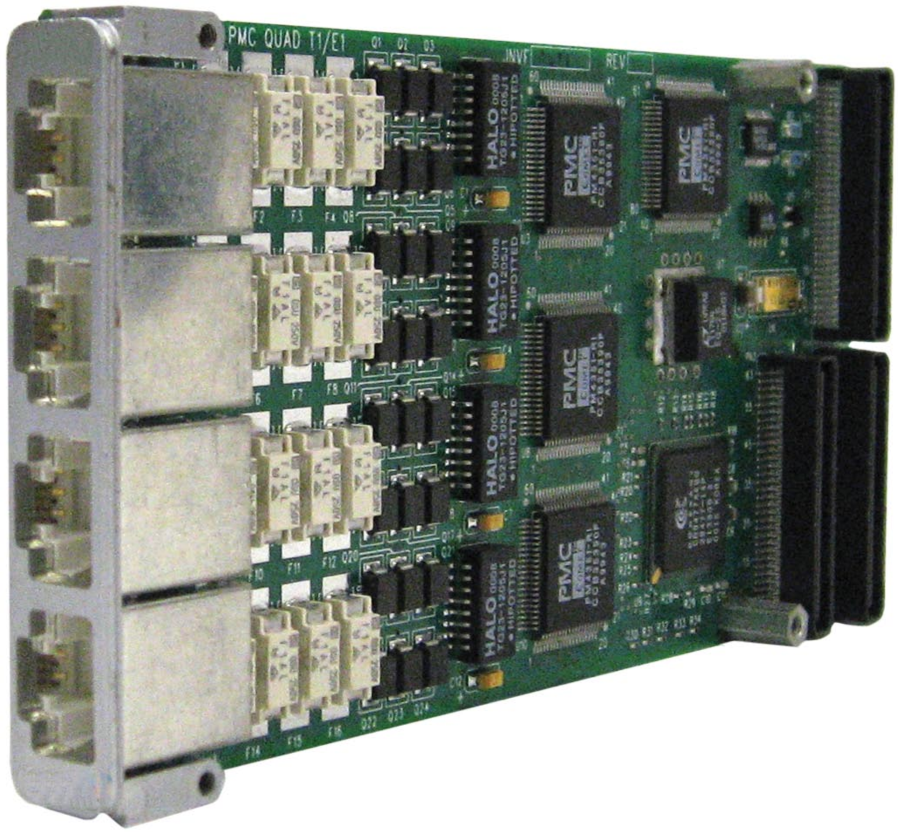

Multi Port T1/E1/J1 PMC

OSS-wanPMC-CxT1E1

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Escondido, CA 92029
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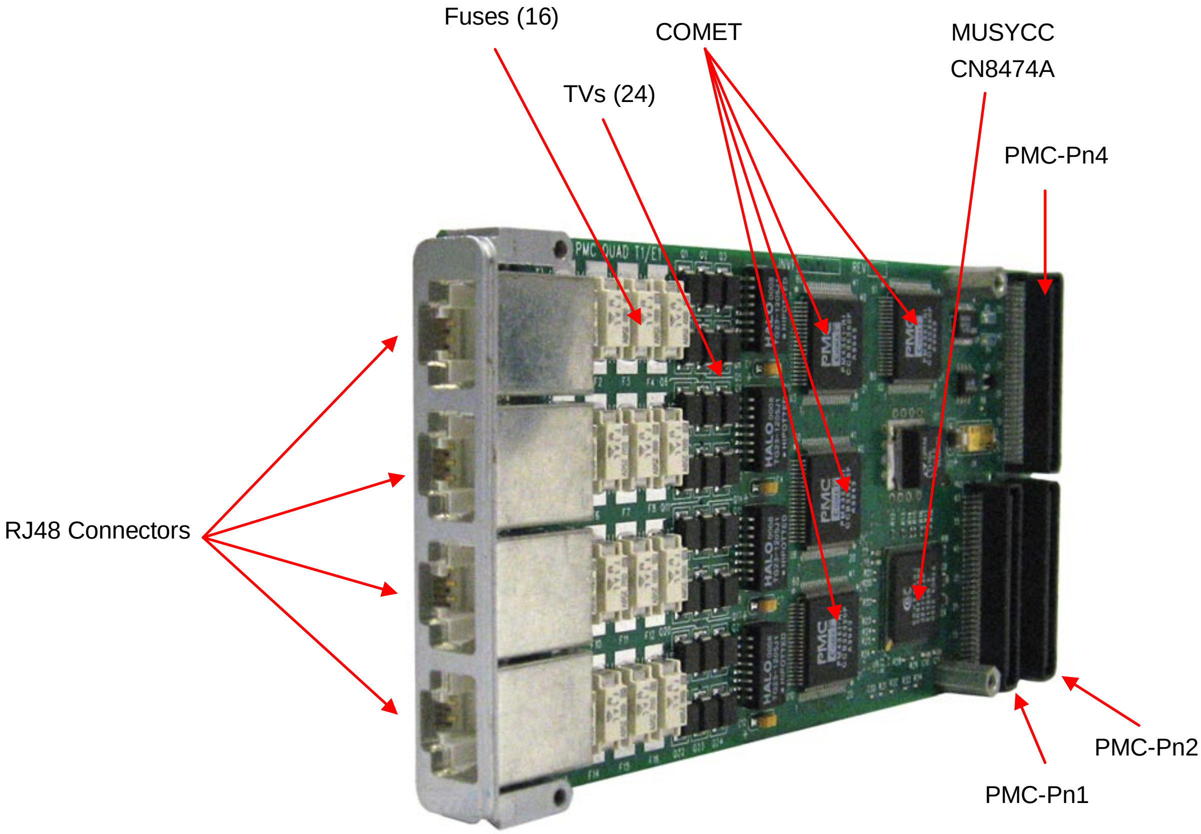
Description

The OSS-wanPMC-CxT1E1 is a mezzanine module designed to the peripheral component interface (PCI) mezzanine card (PMC) specification (IEEE P1386.1/Draft 2.0). This design facilitates communication via four ports at T1/E1/J1 rates (1.544MHz, 2.048MHz, and 1.544MHz, respectively) with other types of systems. Channelized DS0 support is available for T1/E1 or J1. The OSS-wanPMC-CxT1E1can use both SS7or HDLC protocols.



Initial Set-Up

Unpacking Instructions

1. If the carton is damaged when you receive it, request that the carrier's agent be present when you unpack and inspect the equipment.
2. After unpacking, verify that all items listed in the packing list are present.
3. Inspect the equipment for shipping damage.
4. Save all packing material for storage or return shipment of the equipment.
5. For repairs or replacement of equipment damaged during shipment, contact One Stop Systems, Inc. to obtain a Return Materials Authorization (RMA) number and further shipping instructions.

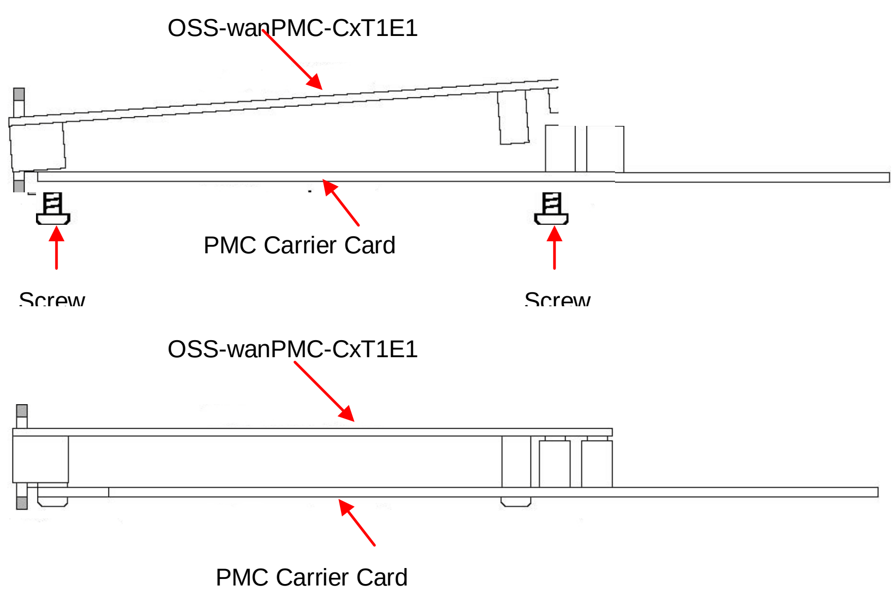
Installation and Removal

1. Power down the host system.
2. Open the chassis according to your system documentation.
3. Let the power supply cool down, if necessary.
4. Remove the host board from the system.
5. Remove the OSS-wanPMC-CxT1E1 from the protective bag, observing proper ESD safety procedures.

Installing the OSS-wanPMC-CxT1E1:

1. Press the OSS-wanPMC-CxT1E1 bezel into the cutout in the PTMC carrier I/O panel. The gasket around the OSS-wanPMC-CxT1E1 bezel makes a tight fit to ensure an electromagnetic seal. Check that the bezel and gasket are pressed firmly into the carrier I/O.
2. Press the OSS-wanPMC-CxT1E1 down onto the carrier so PN1–PN3 plug into JN1–JN3 on the PMC carrier.
3. Install four screws to secure the in place

Installation Diagram



Specifications

Electrical/Mechanical Specifications	
Form Factor:	PCI Telecom Mezzanine Module (PTMC) [5V or 3.3V]
Dimensions (H x L):	5.86 x 2.91 inches (148.8 x 73.9mm)
Front Panel Connectors:	Four RJ48 connectors
Front Panel Indicators:	NONE
Power Consumption (designed to meet the following conditions	
	2.5W maximum @ 3.3V
Operating Environment (designed to meet the following conditions)	
Temperature Range:	-5° to 55°C (23° to 136°F)
Relative Humidity:	20 to 80% non-condensing
Shock:	30g acceleration peak (11ms pulse)
Vibration:	5-17 Hz 0.5" double amplitude displacement; 7-2000Hz, 1.5g acceleration.
Agency Compliance Designed to meet, but not tested	
	NEBS, UL 60950, FCC Class B, CE Mark, CTR13 FCC Part 68, CS-03
MTBF (Telecordia TR-332 Version 6)	
	395,000 hours

Communications Controller

Conexant CN8474A communications controller

The OSS-wanPMC-CxT1E1 uses a Conexant CN8474A communications controller as the HDLC processing engine.

- The CN8474A Multichannel Synchronous Communications Controller (MUSYCC) is an advanced, multichannel, synchronous communications controller that formats and deformats 128 HDLC channels in a single CMOS IC.
- The MUSYCC provides HDLC channels for internetworking applications such as Frame Relay, X.25, Signaling System 7 (SS7), ISDN D-channel signaling, and LAN/WAN data transport.
- Under minimal host supervision, the MUSYCC manages a linked list of channel data buffers in host memory by performing direct memory access (DMA) for the 128 channels, Tx and Rx.

The MUSYCC interfaces with four independent serial data streams, such as T1/E1/J1 signals, and then transfers data across the peripheral component interface (PCI) bus to system memory at a rate of 132 MBps. The wanPMCC4T1E1 will operate for both T1 (1.544MHz) or E1 (2.048MHz). Logical channels can be mapped as any combination of DS0 time slots to support ISDN hyperchannels (Nx64Kbps) or as any number of bits in a DS0 for subchanneling applications (Nx8Kbps)

COMET framer

The four PMC Sierra Framer interface components (PM4351 COMETs) allow the software to select between T1 (100 Ohm), E1 (120 Ohm), and J1 configurations.

I/O

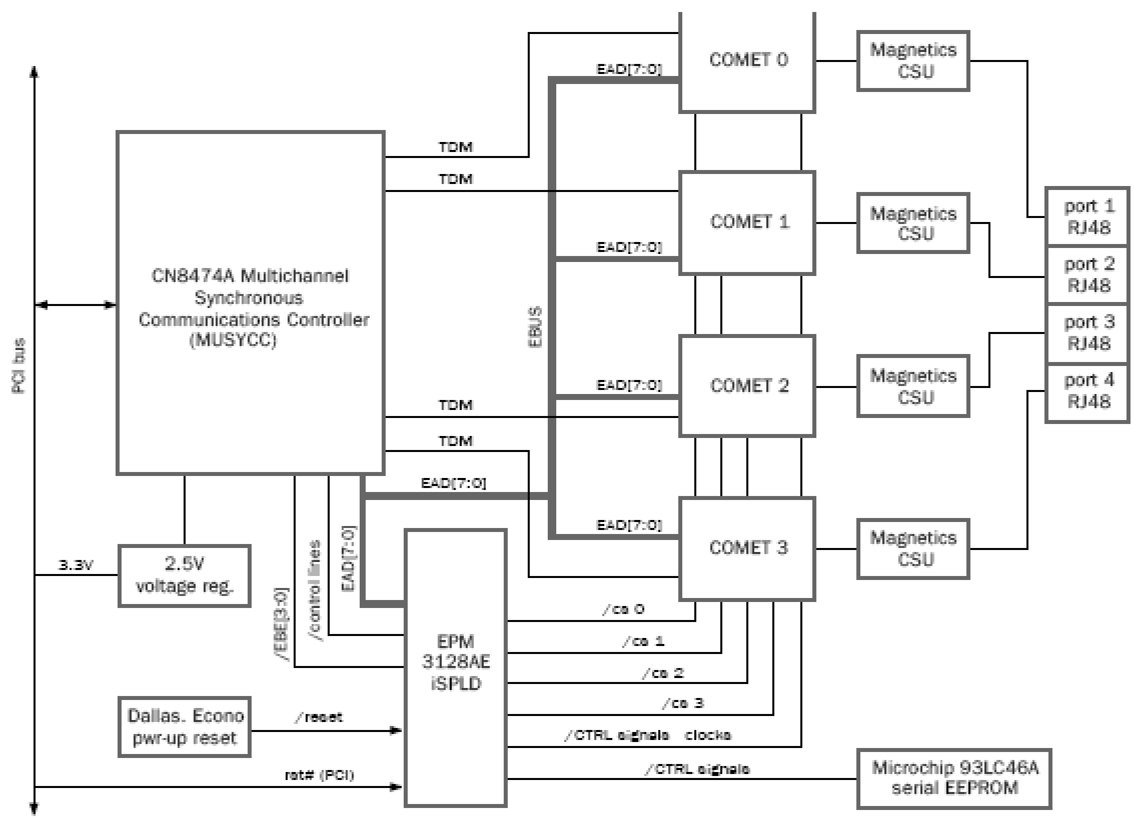
T1/E1/J1 ports

The OSS-wanPMC-CxT1E1 supports four T1/E1/J1 ports. Four onboard COMET chips provide the framer and LIU supporting the four T1/E1/J1 ports. The CSU components reside on the module. The tip and ring for each port are routed to fully shielded RJ48C connectors mounted behind the PMC bezel.

T1/E1/J1 and COMET register settings

COMET register settings impact the TI/E1/J1 pulse waveform and therefore, your telecom (FCC part 68 and CEMark) approval. Register tables are available in the PM4351 COMET COMBINED T1/E1 TRANSCEIVER/FRAMER DATASHEET from PMC-Sierra (PMC-970624). See Chapter 6, In-System Programmable Logic Device (iSPLD), for information on the initialization of the waveform registers and equalizer registers.

Block Diagram



Connectors

The OSS-wanPMC-CxT1E1supports four T1/E1/J1 ports. Four PM4351 COMET chip sets provide the framer and LIU to support the four T1/E1/J1 ports. The CSU components reside on the wanPMC-C4T1E1. The tip and ring for each port are routed to the individual fully shielded RJ48C connector mounted to the PMC bezel.

Connectors (continued)

Communication on the host PCI bus is done across two PMC connectors, **Pn1** and **Pn2.**

The OSS-wanPMC-CxT1E1 can use the **Pn4** connector for rear I/O.

Pn1 32-bit PCI				Pn2 32-bit PCI				Pn4 Rear I/O			
Pin #	Name	Name	Pin #	Pin #	Name	Name	Pin #	Pin #	Name	Name	Pin #
1	TCK	-12V	2	1	+12V	TRST#	2	1			2
3	Ground	INTA#	4	3	TMS	TDO	4	3	TTIP3_PMC		4
5	INTB#	INTC#	6	5	TDI	Ground	6	5	TRING3_PMC		6
7	BUSMODE1#	+5V	8	7	Ground	PCI-RSVD	8	7	TVREF3_PMC		8
9	INTD#	PCI-RSVD	10	9	PCI-RSVD	PCI-RSVD	10	9		/LED0_GRN	10
11	Ground	3.3Vaux	12	11	BUSMODE2#	+3.3V	12	11	RTIP3_PMC		12
13	CLK	Ground	14	13	RST#	BUSMODE3#	14	13	RRING3_PMC		14
15	Ground	GNT#	16	15	+3.3V	BUSMODE4#	16	15		/LED0_YEL	16
17	REQ#	+5V	18	17	PME#	Ground	18	17		/LED1_GRN	18
19	V(I/O)	AD[31]	20	19	AD[30]	AD[29]	20	19	TTIP2_PMC		20
21	AD[28]	AD[27]	22	21	Ground	AD[26]	22	21	TRING2_PMC		22
23	AD[25]	Ground	24	23	AD[24]	+3.3V	24	23	TVREF2_PMC		24
25	Ground	C/BE[3]#	26	25	IDSEL	AD[23]	26	25		/LED1_YEL	26
27	AD[22]	AD[21]	28	27	+3.3V	AD[20]	28	27	RTIP2_PMC		28
29	AD[19]	+5V	30	29	AD[18]	Ground	30	29	RRING2_PMC		30
31	V(I/O)	AD[17]	32	31	AD[16]	C/BE[2]#	32	31		/LED2_GRN	32
33	FRAME#	Ground	34	33	Ground	PMC-RSVD	34	33		/LED2_YEL	34
35	Ground	IRDY#	36	35	TRDY#	+3.3V	36	35	TTIP1_PMC		36
37	DEVSEL#	+5V	38	37	Ground	STOP#	38	37	TRING1_PMC		38
39	Ground	LOCK#	40	39	PERR#	Ground	40	39	TVREF1_PMC		40
41	PCI-RSDV*	PCI-RSVD	42	41	+3.3V	SERR#	42	41		/LED3_GRN	42
43	PAR	Ground	44	43	C/BE[1]#	Ground	44	43	RTIP1_PMC		44
45	V(I/O)	AD[15]	46	45	AD[14]	AD[13]	46	45	RRING1_PMC		46
47	AD[12]	AD[11]	48	47	M66EN	AD[10]	48	47		/LED3_YEL	48
49	AD[09]	+5V	50	49	AD[08]	+3.3V	50	49			50
51	Ground	C/BE[0]#	52	51	AD[07]	PMC-RSVD	52	51	TTIP0_PMC		52
53	AD[06]	AD[05]	54	53	+3.3V	PMC-RSVD	54	53	TRING0_PMC		54
55	AD[04]	Ground	56	55	PMC-RSVD	Ground	56	55	TVREF0_PMC		56
57	V(I/O)	AD[03]	58	57	PMC-RSVD	PMC-RSVD	58	57			58
59	AD[02]	AD[01]	60	59	Ground	PMC-RSVD	60	59	RTIP0_PMC		60
61	AD[00]	+5V	62	61	ACK64#	+3.3V	62	61	RRING0_PMC		62
63	Ground	REQ64#	64	63	Ground	PMC-RSVD	64	63			64

Memory Map

The Expansion Bus (EBus) that carries the data on the OSS-wanPMC-CxT1E1is connected to six byte-wide devices. These devices are the four COMETs, the serial EEPROM, and the iSPLD. The EBus interface uses the lower 20 bits from the PCI address line (AD[19:0]) to construct a byte address for the EBus. Specifically, PCI address lines AD[19:2] are remapped to EBus address lines EAD[17:0].

Device	PCIAddress
COMET 1	xxx80000 Hex
COMET 2	xxx90000 Hex
COMET 3	xxxA0000 Hex
COMET 4	xxxB0000 Hex
SERIAL EEPROM	xxxC0000 Hex
iSPLD	xxxD0000 Hex

Only single D-word (32-bit) PCI operations can be performed when accessing the EBus. Please refer to the N8474/CN8474A specification for more detail. All EBus accesses are on the least significant byte of the PCI bus and are aligned on the 32-bit boundary.

Serial EEPROM

Board serial numbers are stored in a Microchip 93LC46A and packaged in a small outline integrated circuit. This device can hold 1024 bits organized in a 128x8 format. The PCI host reads and writes to this device in a bit serial fashion.

InstructionSB	SB	OP code	EEPROM address bits							Data IN	Data OUT	# CLK cycles
Erase	1	11	A6	A5	A4	A3	A2	A1	A0	--	RDY_/BSY	10
Erase All	1	0	1	0	X	X	X	X	X	--	RDY_/BSY	10
Disable Erase/Write	1	0	0	0	X	X	X	X	X	--	HIGH-Z	10
Enable Erase/Write	1	0	1	1	X	X	X	X	X	--	HIGH-Z	10
Read	1	10	A6	A5	A4	A3	A2	A1	A0	--	D7-D0	18
Write	1	1	A6	A5	A4	A3	A2	A1	A0	D7-D0	RDY_/BSY	18
Write All	1	0	0	1	X	X	X	X	X	D7-D0	RDY_/BSY	18

Extended address bit definitions

Data Bit	Description
0	Data Out
1	Data In
2	Chip Select

Note: Insert a 500ns delay between each bit/write operation

Enable EEPROM

1. Set the chip-select bit and write a one to the EEPROM (serial bit).
2. Keep the chip-select bit set and write the EWEN bit sequence. This includes the don't care address bits.
3. Write the last byte with both the chip-select and data-out bits at zero.

Disable EEPROM

1. Set the chip-select bit and write a one to the EEPROM (serial bit).
2. Keep the chip-select bit set and write the EWDS bit sequence. This includes the don't care address bits.
3. Write the last byte with both the chip-select and data-out bits at zero.

Writing to the EEPROM

1. Enable EEPROM.
2. Set the chip-select bit and write a one to the EEPROM.
3. Keep the chip-select bit set and write the WRITE bits in two writes to the EEPROM.
4. Keep the chip-select bit set and do seven writes indicating the address of interest.
5. Keep the chip-select bit set and do eight writes with the data byte to load. Start with the most significant bit, D7.
6. Write a byte with both the chip-select and data-out bits at zero.
7. Write a byte again with the chip-select bit set.
8. Do two reads of the EEPROM. Discard the first read and check the second read for the data-in bit to be at zero.
9. Periodically read the data-in bit until a one is found.
10. Write a byte with both the chip-select and data-out bits at zero.
11. Disable EEPROM.

Reading from the EEPROM

1. Set the chip-select bit and write a one to the EEPROM.
2. Keep the chip-select bit set and write the READ bits in two writes to the EEPROM.
3. Keep the chip-select bit set and do seven writes indicating the address of interest.
4. Keep the chip-select bit set and do nine reads. Discard the first read. The eight remaining reads take the data from the data-in bit and shift it to the least significant bit position. Data is read starting from most significant bit position, D7. (Remember the data-in bit is at position one.)
5. Write a byte with both the chip-select and data-out bits at zero.

Initialization

The OSS-wanPMC-CxT1E1must be reset and initialized before it can be programmed. This section contains the necessary code to reset and initialize the waveform and the equalizer registers.

Reset Functions

After powerup, a Dallas DS1817 chip generates a reset that forces all components on the OSS-wanPMC-CxT1E1into a reset state that terminates after 150ms. A second reset source is the PMC's #RST pin from the PCI or VME host.

The host must configure the MUSYCC as a PCI master; this allows the MUSYCC to access host memory addresses. The host also must write to the function 1 PCI configuration command register, enabling access to the OSS-wanPMC-CxT1E1EBus space.

The following steps outline the sequence of events to bring up the board after a reset condition.

1. Map function 0 and function 1 into the PCI's memory address space. Each function requires at least 1 megabyte of memory space.
2. Enable memory accesses onto the PMC's space.
3. Write to the Global Configuration Descriptor in the MUSYCC that sets up the access time and enables the EBus for individual accesses.
4. Depending on how you want the board configured, write to the MCLK register next to configure which ports are E1 and which are T1. Then write to the master clock select register (MCSR) to define which port(s) should be master.
5. Initialize the COMETs based on the MCSR setting.
6. Initialize the MUSYCC to support your specific requirements.

COMET and MUSYCC Initialization

The COMETs and the MUSYCC must be initialized so that the data being clocked in and out of the MUSYCC occurs on the proper edges. The following settings serve both master and slave clock modes in the COMET. These lines of code initialize the clock edge to strobe data out of the MUSYCC, out of the COMET, and on the receive side as well.

COMET configuration for the powerup default settings of the MCLK and MCS registers as master

```
Register 0x30; BRIF Configuration
NXDSO[1-0] = 0
CMODE = 0      BRCLK as an output

DE = 0: Use the falling edge of BRCLK
FE = 0: Use falling edge of BRCLK

Register 0x31; BRIF Frame Pulse Configuration
FPMODE = 0     BRFP as an output

Register 0x40; BTIF Configuration
NXDSO[1,0] = 0
CMODE = 1      BTCLK as an input

DE = 1: Use the rising edge of BTCLK
FE = 1: Use rising edge of BTCLK

Register 0x41; BTIF Frame Pulse Configuration
FPMODE = 1     BTFP as an input
```

COMET configuration for the slave setting

```
Register 0x30; BRIF Configuration
NXDSO[1,0] = 0
CMODE = 1      BRCLK as an input

DE = 0: Use the falling edge of BRCLK
FE = 0: Use falling edge of BRCLK

Register 0x31; BRIF Frame Pulse configuration
FPMODE = 1     BRFP as an input

Register 0x40; BTIF configuration
NXDSO[1,0] = 0
CMODE = 1      BTCLK as an input

DE = 1: Use the rising edge of BTCLK
FE = 1: Use rising edge of BTCLK

Register 0x41; BTIF Frame Pulse Configuration
FPMODE = 1   BTFP as an input
```

Note: NXDSO[1,0] This is the recommended setting, full frame. For other configurations, we recommend configuring the MUSYCC for that specific mode of operation.

Serial EEPROM

A 500ns delay is necessary for both read and write cycles of the serial EEPROM. Since the MUSYCC's data cycle time is approximately 300ns, the algorithm by which data is read from the serial EEPROM in a timely fashion will be as follows:

- The EEPROM must go through an EEPROM enable command at least once and is not disabled until the operation is complete. Only PCI single writes and reads can be used.
- A minimum of 500ns delay must exist between each single host access to and from the serial EEPROM.

Global configuration descriptor

BLAPSE[2-0] = 7
ECKEN = 1   Enable PCI clock to the EBUS
MPUSEL = 0
ALAPSE[1-0] = 3
ELAPSE[2-0] = 7
PORTMAP[1-0] = 0

Port configuration descriptor

ROOF_EDGE = 0   It is not used on this product
RSYNC_EDGE = 1   Rising edge
RDAT_EDGE = 1   Rising edge
TSYNC_EDGE = 1   Rising edge
TDAT_EDGE = 0   Falling edge

In-System Programmable Logic Device (iSPLD)

The In-System Programmable Logic Device (iSPLD) contains all of the necessary logic required by the CN8474A to communicate with its peripheral components. The iSPLD serves two purposes:

1. As a general logic device, supplying correct signal timing and address decoding for chip selects to the COMETs and EEPROM.
2. To provide registers to control the crystal routing and BRCLK routes to and from the COMETs and MUSYCC.

The iSPLD is an Altera EPM3256AE and serves the following logic functions:

- T1/E1/J1 clock routing to all COMETs
- COMET interrupts
- Serial EEPROM control
- COMET control
- LED control
- Master clock connections
- Reset functions

iSPLD registers, base address (EAD) = 0xD0000

Address offset	Register type	Function
0x0	Write/read	MCSR
0x4	Write/read	MCLK register
0x8	Write/read	LED register
0xC	Read only	Interrupt register

iSPLD Control Functions

Write/read operations executed by the CN8474A via its EBus are translated to the appropriate timing for the PMC4351. The iSPLD decodes the address and generates the chip-select levels for each of the COMETs

Master Clock Select Register

Any or all of the COMETs can provide the clock for data synchronization. The host, via the MCSR, decides which COMET provides the clock. At reset, each COMET provides the clock for its port and must be configured as the master. In modes other than default or reset, one port is assigned the master with the iSPLD routing this clock to the remaining COMETs and MUSYCC.

The MCSR in the iSPLD can be written to and read by the PCI host. Immediately after powerup or host reset this register is initialized to all zeros. By default, COMET 1 serves to provide the master clock. The host may then select the clocking needs via the MCSR. See Master Clock Registers Table on next page for information about the MCSR and clocking information.

Master Clock Registers (MCSR)

MCSR	Clock Source
00 Hex	All ports (COMETs) use their individual backplane clock as the clocksource used by their respective MUSYCC ports. NOTE: All COMETs must be initialized in master mode. COMET 1 provides clocking to MUSYCC port 0. COMET 2 provides clocking to MUSYCC port 1. COMET 3 provides clocking to MUSYCC port 2. COMET 4 provides clocking to MUSYCC port 3.
01 Hex	Port 1 (COMET 1) uses its backplane clock to provide the source clocking for all other COMETs including the MUSYCC ports. NOTE: COMET 1 must be initialized in master mode. COMETs 2, 3, and 4 must be initialized in slave mode.
02 Hex	Port 2 (COMET 2) uses its backplane clock to provide the source clocking for all other COMETs including the MUSYCC ports. NOTE: COMET 2 must be initialized in master mode. COMETs 1, 3, and 4 must be initialized in slave mode.
03 Hex	Port 3 (COMET 3) uses its backplane clock to provide the source clocking for all other COMETs including the MUSYCC ports. NOTE: COMET 3 must be initialized in master mode. COMETs 1, 2, and 4 must be initialized in slave mode.
04 Hex	Port 4 (COMET 4) uses its backplane clock to provide the source clocking for all other COMETs including the MUSYCC ports. NOTE: COMET 4 must be initialized in master mode. COMETs 1, 2, and 3 must be initialized in slave mode.

Note: The backplane clock is the clock between the COMET and the MUSYCC.

The COMET decides if the backplane clock is sourced by the central office or the onboard oscillator

Master Clock register

The framers require a MCLK that can be either T1 (1.544MHz) or E1 (2.048MHz). Two onboard oscillators are provided to be the source of those clocks. The MCLK register is used to select between the two oscillators. The MCLK register is a write/read register set to default to zero after powerup or system reset. The table below defines the state of the MCLK for each framer based on the register setting for MCLK register.

MCLK Register - Address Offset =1 Write Read				
	Port 4	**Port 3**	**Port 2**	**Port 1**
Bits 7–4	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Reserved	0 – T1	0 – T1	0 – T1	0 – T1
	1 – E1	1 – E1	1 – E1	1 – E1

LED register

There are nine LEDs mounted on the back of the board. Eight LEDs are programmable and can be used for AIS and RAI alarms. The ninth LED is the power LED. The table below defines each bit in the LED register

LED Register – Address Offset = 2 – Write / Read							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CR8 Yellow	CR9 Green	CR6 Yellow	CR7 Green	CR4 Yellow	CR5 Green	CR2 Yellow	CR3 Green

0 = OFF

1 = ON

The signals that drive the LEDs are also sourced to the connector PMC-PN4. Users of the PMC-PN4 connector can display the state of the LEDs on another display panel. This allows display of RAI and AIS for each port or development indication.

Interrupts

The MUSYCC requires the use of PCI signals INTA# and INTB#.. INTA# is driven by the MUSYCC to indicate a MUSYCC layer-2 interrupt condition to the PCI host processor.. INTB# is driven by the MUSYCC to notify the PCI host processor of an interrupt pending from the EBus. Interrupts from the COMETs are latched in a register resident in the iSPLD. The interrupts from the COMETs are logically OR-ed to generate an interrupt to the MUSYCC. The MUSYCC transfers this interrupt from the EBus to the PCI INTB# pin when enabled in the Global Configuration Descriptor. The PCI host processor reads the interrupt register to determine which device was responsible for the interrupt. These bits are direct links from each COMET. They are cleared only when that COMET.s interrupts have been cleared

Interrupt Register – Address Offset = 3 – Read Only							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
X	X	X	X	COMET 4	COMET 3	COMET 2	COMET 1

0 = No interrupt

1 = Interrupt pending

X = Reserved (don.t care)

The appropriate COMET clears the interrupt bit when the interrupt is serviced

Power LED

The ninth LED is the power LED. This bicolor LED indicates the status of the 2.5V regulator. Table 6-6 defines its states. The power LED is not software accessible.

Power LED Bicolor	2.5 Volt Status
Green	Power is OK
Red	Power is BAD

JTAG

The OSS-wanPMC-CxT1E1has six components that are capable of JTAG functionality. Five of these components are connected to the JTAG interface pins in accordance with the PMC specification. JTAG connectivity begins with the PMC connector and serpentines through the five devices as shown below.

The following components will support JTAG functions:

JTAG	CN8474A6	Comet # 1	Comet # 1	Comet # 1	Comet # 1	EPM3256A
PMC connector	yes	yes	yes	yes	yes	no

The EPM3256A is capable of JTAG functionality; however, it is not connected to the JTAG chain. A separate connector that is used primarily for programming the EPM3256A can also be used to JTAG-test the iSPLDdevice.

Note: Framer TDO signals will require 10K pull up resistors

Limited Warranty

One Stop Systems warrants this product to be free of defects in material and workmanship for an initial period of two years from date of delivery to the original purchaser from One Stop Systems.

During this period, One Stop Systems will, at its option, repair or replace this product at no additional charge to the purchaser, except as set forth in this warranty agreement.

One Stop Systems will, at its option, repair or replace this product at no additional charge to the purchaser, if the defect is related to the One Stop Systems manufactured product, such as a power supply, backplane, other chassis components or CPUs. One Stop Systems is not liable for any defects in material or workmanship of any peripherals, products or parts, which One Stop Systems does not design or manufacture. However, One Stop Systems will honor the original manufacturer's warranty on these products. One Stop Systems will analyze the defective component and the customer will be charged in the following instances:

No problem found: $75 (U.S. dollars).

Damage: Parts and labor at $75 per hour with a $100 minimum charge (U.S. dollars). Receipt of damaged goods voids the One Stop Systems warranty.

Repair parts and replacement products will be furnished on an exchange basis and will be either new or reconditioned. All replacement parts and products shall become the property of One Stop Systems, if such parts or products are provided under this warranty agreement. In the event a defect is not related to the One Stop Systems manufactured product, One Stop Systems shall repair or replace the defective parts at the purchaser's cost and deliver the defective parts to the purchaser.

This limited warranty shall not apply if the product has been misused, carelessly handled, defaced, modified or altered, or if unauthorized repairs have been attempted by others. The above warranty is the only warranty authorized by One Stop Systems and is in lieu of any implied warranties, including implied warranty of merchantability and fitness for a particular purpose. In no event will One Stop Systems be liable for any such damage as lost business, lost profits, lost savings, downtime or delay, labor, repair or material cost, injury to person or property or any similar or dissimilar consequential loss or damage incurred by the purchaser, even if One Stop Systems has been advised of the possibility of such losses or damages.

In order to obtain warranty service, the product must be delivered to the One Stop Systems facility, or to an authorized One Stop Systems service representative, with all included parts and accessories as originally shipped, along with the proof of purchase and a Returned Merchandise Authorization (RMA) number.

The RMA number is obtained, in advance, from One Stop Systems Customer Service Department and is valid for 30 days. The RMA number must be clearly marked on the exterior of the original shipping container or equivalent. Purchaser will be responsible and liable for any missing or damaged parts. Purchaser agrees to pay for shipping charges one way, and to either insure the product or assume the liability for loss or damage during transit. Ship to:

One Stop Systems
ATTENTION: RMA REPAIR DEPARTMENT
RMA ####
2235 Enterprise Street, Suite 110
Escondido, CA 92029
www.onestopsystems.com
2235 Enterprise Street, Suite 110 • Escondido, CA 92029 • Tel (760) 745-9883 • Fax (760) 745-9824