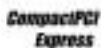


Single Port Channelized T3PMC



OSS-wanPMC-xT3E3



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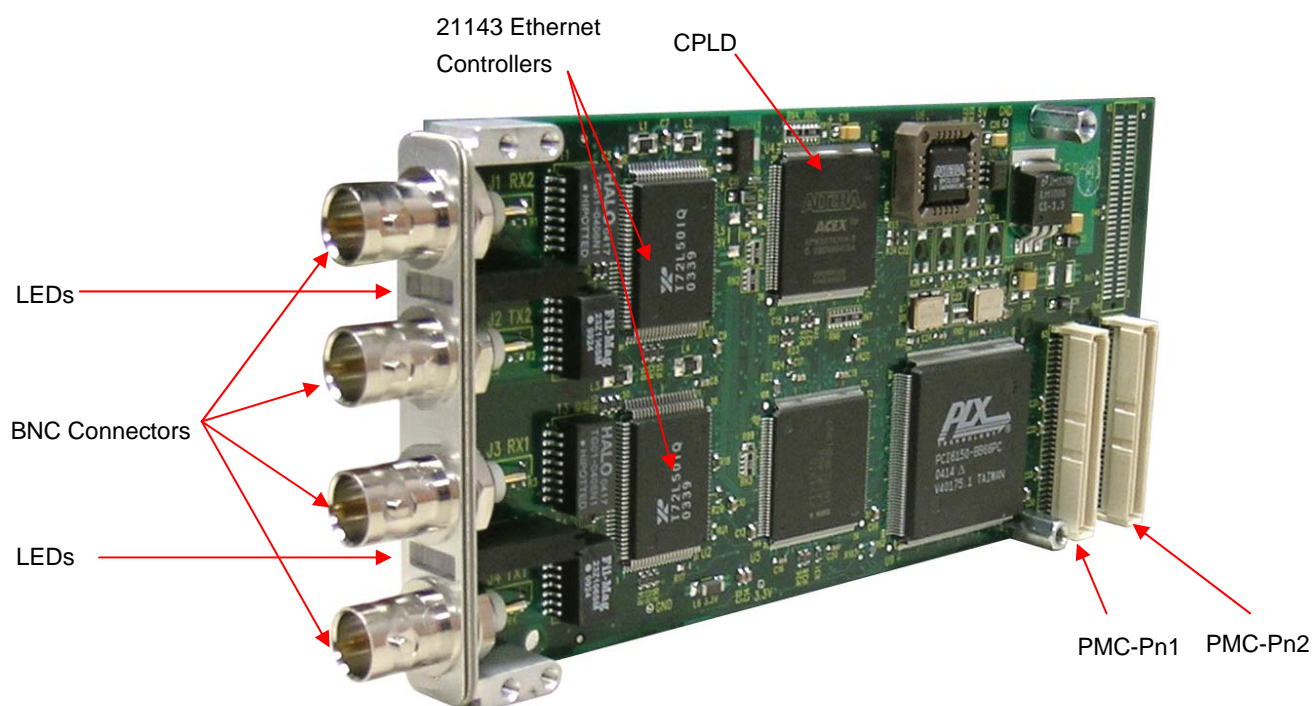
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Description

The OSS-wanPMC-xT3E3 is a PCI Mezzanine Card (PMC) board with two T3/E3 ports. The T3 format complies with the ANSI T1.404-1994 standard and the E3 format complies with the ITU-T G.751 and ITU-T G.832 standards.

Attached to the OSS-wanPMC-xT3E3 PCB is a PMC bezel with a custom stamp out to accommodate four T3/E3 BNC connectors and eight bi-color LEDs. The OSS-wanPMC-xT3E3 offers two ports of either T3 or E3 connectivity providing clear-channel communication. Frames are transferred between the T3/E3 ports and a 33-MHz/32-bit host PCI bus. The OSS-wanPMC-xT3E3 also supports three modes of operation: HDLC payload mode, transparent payload mode, and raw mode.

In addition, rear I/O support on the PMC Pn4 connector is provided via software-controlled FETs switches where the TIPS and RINGS of the Line Interface Unit (LIU) are routed to the connector.



Initial Set-Up

Unpacking Instructions

1. If the carton is damaged when you receive it, request that the carrier's agent be present when you unpack and inspect the equipment.
2. After unpacking, verify that all items listed in the packing list are present.
3. Inspect the equipment for shipping damage.
4. Save all packing material for storage or return shipment of the equipment.
5. For repairs or replacement of equipment damaged during shipment, contact One Stop Systems, Inc. to obtain a Return Materials Authorization (RMA) number and further shipping instructions.

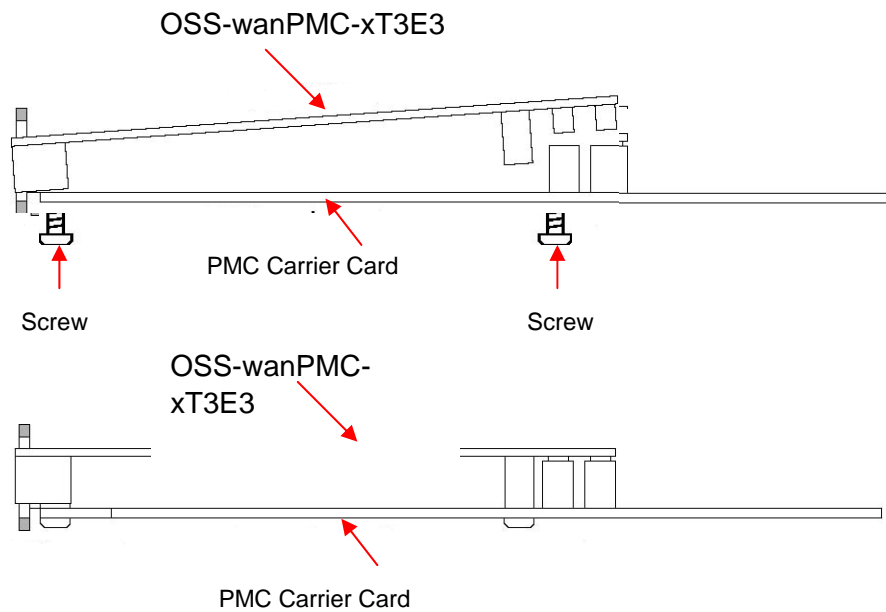
Installation and Removal

1. Power down the host system.
2. Open the chassis according to your system documentation.
3. Let the power supply cool down, if necessary.
4. Remove the host board from the system.
5. Remove the OSS-OSS-wanPMC-xT3E3 from the protective bag, observing proper ESD safety procedures.

Installing the OSS-wanPMC-xT3E3:

1. Press the OSS-wanPMC-xT3E3 bezel into the cutout in the PMC carrier I/O panel. The gasket around the OSS-OSS-wanPMC-xT3E3 bezel makes a tight fit to ensure an electromagnetic seal. Check that the bezel and gasket are pressed firmly into the carrier I/O.
2. Press the OSS-wanPMC-xT3E3 down onto the carrier so PN1–PN2 plug into JN1–JN2 on the PMC carrier.
3. Install four screws to secure the in place

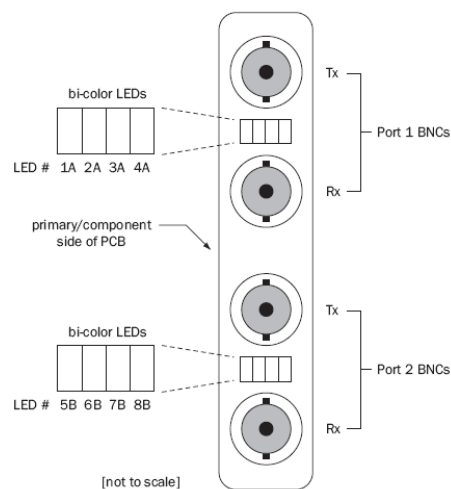
Installation Diagram



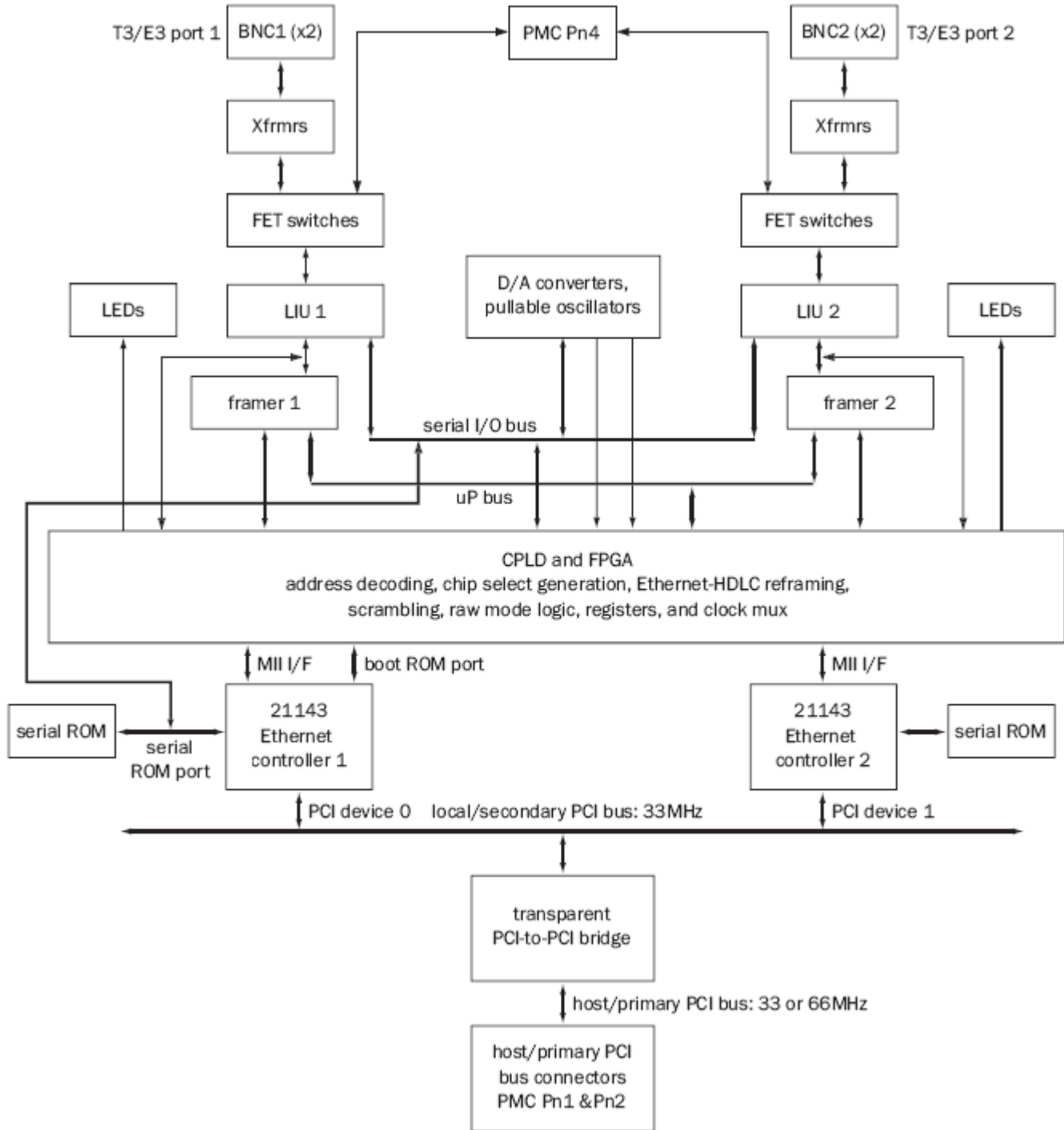
Specifications

Electrical/Mechanical Specifications	
Form Factor:	PCI Mezzanine Card (PMC) [5V or 3.3V]
Dimensions (H x L):	5.86 x 2.91 inches (148.8 x 73.9mm)
Front Panel Connectors:	Four BNC Connectors
Front Panel Indicators:	Two sets of 4 Bi-color LEDs
Power Consumption (designed to meet the following conditions)	
	7.5W maximum @ 3.3V
Operating Environment (designed to meet the following conditions)	
Temperature Range:	-5° to 55°C (23° to 136°F)
Relative Humidity:	20 to 80% non-condensing
Shock:	30g acceleration peak (11ms pulse)
Vibration:	5-17 Hz 0.5" double amplitude displacement; 7-2000Hz, 1.5g acceleration.
Agency Compliance Designed to meet, but not tested	
	NEBS, UL 60950, FCC ClassA, CE Mark, VCCI
MTBF (Telecordia TR-332 Version 6)	
	>200,000 hours

Front Panel



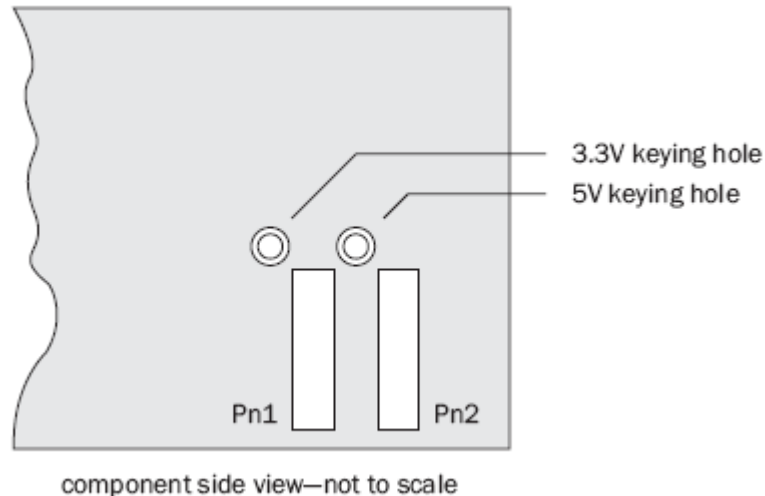
Block Diagram



Keying

The OSS-wanPMC-xT3E3 can be operated in a 5V or 3.3V signaling environment. The signaling environment is determined by the voltage on the PCI VIO pins and is host-specific.

When installing the card on a host, the voltage coding key must be installed in accordance with the host requirements. If the Host is capable of accommodating both 3.3 and 5 volt signaling, then the 3.3 volt signaling is preferred



Power

Power is supplied to the OSS-wanPMC-xT3E3 by the carrier board. Current is drawn from the 5V and 3.3V power pins. The tolerance on the 5V and 3.3V supply is $\pm 10\%$ in accordance with the PCI Local Bus Specification

PCI-PCI Bridge Module

The OSS-wanPMC-xT3E3 uses any of the following three components, in the 208-pin PQFP package, for the PCI-to-PCI bridge:

- Texas Instruments' PCI2050APDV or
- HiNT HB4 or
- Intel SB21150BC

The PCI bridge supports a 32-bit, 33/66-MHz primary (host) PCI bus and 32-bit, 33/66-MHz secondary (local) PCI bus. In this design only the 33-MHz capability will be used on the secondary bus. The PCI bridge can operate as a PCI Master or Slave for memory and I/O accesses on a 33-MHz, 32-bit secondary (local) PCI bus. The bridge does not support interrupt handling and routing. This is done externally in the CPLD.

Primary (Host) PCI Bus

Since the PCI bridge can support either 33MHz or 66MHz, the M66EN signal from the PMC connector is used as an input to determine the host PCI clock speed.

Resets

The following types of resets are available:

- Power-on reset from the primary PCI bus, which resets the entire board including the PCI bridge.
- Host accessible reset allowing the host on the PCI bus to reset the board's local PCI bus, which includes the Ethernet Controllers, the DS3 framers, LIUs, and the FPGA via a register bit in the PCI bridge.
- Host accessible reset enabling the host to reset each peripheral device separately via bits in the Static Reset Register (SRR) and Pulse Reset Register (PRR).

PCI host controllable indicators and miscellaneous indicators

There are eight green/yellow bi-color LEDs located at the bezel of the OSS-wanPMC-xT3E3 (see Figure 3-2) that are controllable by software via the two LED Registers (LEDRA and LEDRB) implemented in the CPLD). At powerup, all front panel LEDs are off. There is also a green “Program OK” LED located along the top edge of the PCB on the secondary side of the PCB. When this LED is lit, the FPGA has been configured.

PCI interrupt assignments

Since the PCI bridge does not support interrupts, the interrupts are routed from the peripheral devices to the host PCI bus via the CPLD. The table below shows the OSS-wanPMC-xT3E3's interrupt assignments and the possible sources of the PCI interrupts.

PCI Interrupt Line	Sources of the PCI Interrupt
INTA#	Ethernet Controller 1 Interrupt Framer 1 Interrupt Port 1 Line Code Violation (LCV) Limit Exceeded Interrupt AMI Signal not detected (DMO asserted) by LIU 1 Receive Loss of Lock (RLOL) state from LIU 1 Receive Loss of Signal (RLOS) state from LIU 1
INTB#	Ethernet Controller 2 Interrupt Framer 2 Interrupt Port 2 Line Code Violation (LCV) Limit Exceeded Interrupt AMI Signal not detected (DMO asserted) by LIU 2 Receive Loss of Lock (RLOL) state from LIU 2 Receive Loss of Signal (RLOS) state from LIU 2
INTC#	Not Used
INTD#	Not Used

Since a single interrupt is generated to the PCI host for each port, the host can determine the source of the interrupt by reading the Interrupt Control and Status Registers. There is a corresponding interrupt enable bit for each interrupt source either disabling or enabling any interrupt or status indicator as a source to the PCI interrupts. There are two interrupt enable registers, one for each port.

Busmode Pins

Since OSS-wanPMC-xT3E3 supports only the PCI bus protocol at the PMC connectors, the BUSMODE1# pin is asserted LOW for two reasons only; (1) to indicate its presence to the host, and (2) to indicate that it is capable of performing PCI Bus protocol (see Table below). The OSS-wanPMC-xT3E3 responds within ten PCI clock cycles after detecting the state of BUSMODE[4:2]# pins.

BUSMODE[4:2]# state (input)	Mode	BUSMODE1# output state	Response explanation
000	“Card Present” test.	0	“Card Present” mode. No bus protocol is used and card is held in reset
001	Return Card Present if PCI capable and uses PCI protocol.	0	Capable of performing PCI protocol.
All other states	-	1	Card held in reset.

PMC debug support (JTAG).

The OSS-wanPMC-xT3E3 makes its JTAG signals available on the Pn1 and Pn2 connector pins (TCK, TRST#, TMS, TDI, and TDO) as specified in the PMC specification. The OSS-wanPMC-xT3E3 includes the following devices in its JTAG chain so that complete JTAG testing of OSS-wanPMC-xT3E3 can be performed: PCI bridge (21150), Ethernet controllers (21143s), 3.3-volt DS3 Framers (XRT72L50s), the CPLD (CPM3256), the FPGA (EP1K30), and the configuration EEPROM (EPC2), which can be bypassed. If the configuration device is a one-time programmable device or not installed, a JTAG “jumper” (zero-ohm resistor) must be installed. Since devices relating to port 2 can be depopulated for a single port product, two separate JTAG “jumpers” must be installed to complete the JTAG chain when Ethernet controller 2 and framer 2 are not installed. JTAG jumpers must be installed for each of the DS3 framers when the 5-volt non-JTAG devices are installed. These “jumpers” are not installed when using the 3.3-volt devices, which support JTAG.

Secondary (Local) PCI Bus

The Ethernet controllers operate with a PCI clock speed of 33MHz; therefore the secondary PCI bus speed is set accordingly. This is set by connecting the S_M66ENA pin of the PCI bridge to ground via a pulldown resistor.

The PCI bridge is the PCI arbiter on the secondary PCI bus. The PCI bridge’s internal arbiter is enabled by grounding its /S_CFN pin through a pulldown resistor.

Secondary PCI bus peripherals: Ethernet controllers

Only two peripherals are connected to the local PCI bus: both are Ethernet controllers—one for each T3/E3 port. The Ethernet controller selected is Intel’s 21143TD 10/100 LAN Controller in the 144-pin LQFP package. The 21143 is used to transfer data between the T3/E3 line and memory. It implements many features such as large internal FIFOs and cache line reads/writes to achieve fast data transfer.

Ethernet controller memory

Upon reset, each Ethernet controller is initialized via its own external serial EEPROM. The EEPROM is programmed per the Intel Serial ROM format during manufacturing with the following information:

- Serial number of the board embedded in the IEEE Network address (MAC address) location
- PCI Subsystem ID (0009H = OSS-wanPMC-xT3E3)
- PCI Subsystem Vendor ID (1176H = OSS)

All other memory locations except the checksum are free for use by the customer.

Microchip’s 93LC46B Serial EEPROM is used in this design. Although this device can operate with supply power as low as 2.5 volts, it operates at 3.3 volts in this design. It is a 1K-bit device organized as 64 x 16 bits in a SO-8 package. The access time for this device is 400nsec.

Ethernet MII port

The MII/SYM port is used to transmit and receive Ethernet frames from the DS3 framer via the FPGA. Since this interface has a 4-bit data interface (one for transmit and one for receive), the MII transmit/receive clocks can be ¼ to ½ the T3/E3 clock rate.

Ethernet boot ROM and serial ROM ports. The boot ROM port is used to access the microprocessor I/O devices. The serial ROM port is used to access the serial I/O devices.

Ethernet controller clocks

The clock for the PCI interface is generated by the secondary PCI interface of the PCI bridge. This is 33.33MHz clock.

The XTAL1 input pin must toggle for the controller’s internal state machines to operate during configuration. Therefore, this pin is driven with a clock that is ½ the T3 rate (22.368MHz) or ½ the E3 rate (17.814MHz). The transmit and receive clocks for the Ethernet portion of the 21143 are generated by the FPGA. This clock can either be ¼ of the T3/E3 port rate (11.184MHz for T3 or 8.592MHz for E3) or ½ of the port rate (22.368MHz for T3 or 17.184MHz for E3).

IDSEL

The following table defines the IDSEL for each PCI capable component, its corresponding secondary (local) PCI address bit, its PCI device number, its REQ/GNT signal level at the PCI bridge, and its interrupt assignment on the host PCI bus.

IDSEL Device	Secondary PCI Address Bit	PCI Device Number	REQ/GNT Signal Level	Interrupt Assignment
Ethernet controller 1	16	0	0	INTA#
Ethernet controller 2	17	1	1	INTB#

Local PCI address space map

There are three possible masters on the OSS-wanPMC-xT3E3's local PCI bus: the two Ethernet controllers and the PCI-to-PCI bridge. The Ethernet controllers have access to the host PCI bus memory, allowing them to do DMA transfers.

I/O Peripheral Module

The I/O peripheral module consists of devices connected to either the microprocessor I/O bus or the serial I/O bus. The host can access these devices via Ethernet controller 1 (21143). The 21143's boot ROM port is used to access the microprocessor I/O devices; the serial ROM port is used to access the serial I/O devices.

Microprocessor I/O Bus Peripherals

The 21143's CSR9 and CSR10 registers must be set to access devices on its boot ROM port. All peripherals and registers on this bus are accessed on long-word boundaries.

Region	Address Range	Description
Port 1 Control and Status	0x0000	Port 1 Control Register A
	0x0004	Port 1 Control Register B
	0x0008	Port 1 LCV Count Register
	0x000C	Port 1 LCV Threshold Register
	0x0010	Port 1 Payload Fill Register (Raw/Transparent Modes)
Port 2 Control and Status	0x0080	Port 2 Control Register A
	0x0084	Port 2 Control Register B
	0x0088	Port 2 LCV Count Register
	0x008C	Port 2 LCV Threshold Register
	0x0090	Port 2 Payload Fill Register (Raw/Transparent Modes)
Port 3	0x0100 – 0x017C	Reserved for Port 3 Control & Status Registers
Port 4	0x0180 – 0x01FC	Reserved for Port 4 Control & Status Registers
Miscellaneous Control and Status	0x0200	Board ID / FPGA Programming Status Register
	0x0204	FPGA Version Register
	0x0208 – 0x07FC	Reserved

Region	Address Range	Description
Port 1 Framer	0x0800	Port 1 Framer Operating Mode Register
	0x0804	Port 1 Framer I/O Control Register
	0x0808 – 0x0CD4	Remaining Port 1 Framer Registers
	0x0CD8 – 0x0FFF	Reserved
Port 2 Framer	0x1000	Port 2 Framer Operating Mode Register
	0x1004	Port 2 Framer I/O Control Register
	0x1008 – 0x14D4	Remaining Port 2 Framer Registers
	0x14D8 – 0x1FFF	Reserved
Miscellaneous Control and Status 0x2000 – 0x2FFF	0x2000	Serial Chip Select Register
	0x2004	Static Reset Register
	0x2008	Pulse Reset Register
	0x200C	FPGA Reconfiguration Register
	0x2010	LED Register A
	0x2014	LED Register B
	0x2018	Port 1 LIU Control and Status Register
	0x201C	Port 2 LIU Control and Status Register
	0x2020	Port 1 Interrupt Enable Register
	0x2024	Port 2 Interrupt Enable Register
	0x2028 – 0x2FFF	Reserved
Reserved	0x3000 – 0x8FFF	Reserved

DS3/E3 framer

The framer has a 9-bit address bus and 8-bit data bus. The boot ROM address/data bus of Ethernet controller 1 is demultiplexed and the address is shifted in the CPLD. The result is presented to the framer as a multiplex address/data bus. Note: Upon power-up, the framer defaults to E3 mode. Therefore, for T3 networks the framer must be configured to DS3 mode.

The LIU and framer both default to encoding/decoding either B3ZS (for DS3) or HDB3 (for E3). Therefore, after power-up, the encoder/decoder in either the framer or LIU must be turned off. Note that in RAW mode, encoding must be done by the LIU. (Decoding may be done in the framer or LIU.) Configure the framer to sample data received from the LIU on the falling edge of the RxLinkClk signal. By default the LIU updates the RxPOS and RxNEG data signals on the rising clock edge.

FPGA Registers

The Board ID Register and the Port Control Registers are implemented in the FPGA while the FPGA register selects are generated by the CPLD

CPLD Registers

All Miscellaneous Control/Status Registers except for the Board ID Register are implemented in the CPLD. The CPLD generates the chip selects for all devices (parallel and serial).

Serial I/O Bus Peripherals

The 21143's CSR9 register must be set to access devices on its serial ROM port. In addition, the serial I/O bus peripherals are accessed by setting the desired serial device in the Serial Chip Select Register. The register bits and Ethernet controller 1's serial ROM chip select are AND'd together to generate the actual chip select to a particular device. The remaining serial ROM signals (clock, data in, and data out) of Ethernet controller 1 are routed directly to all of serial devices: the LIUs and DACs. Note: The SCSR powers up with Serial ROM 1's chip select enabled so that Ethernet Controller 1 can read the ROM at power-up.

DS3/E3 Line Interface Unit

The Line Interface Unit (LIU) used for each port is EXAR's XRT7300 in the 44-pin TQFP package. The LIU supports both DS3 and E3 networks.

The LIU is operated in Host mode, that is, its operation is controlled by internal register settings. The registers are accessible via the Serial I/O bus using a 16-bit serial string. The 16-bit string is broken into three parts: 1 bit for read/write, 7 bits for address, and 8 bits for data. See the XRT73(L)00 data sheet for register details and the format of the serial data

After powerup, the LIU defaults to DS3 and bi-polar modes. For E3 networks, the LIU must be reconfigured for E3 mode.

The LIU and framer both default to encoding/decoding either B3ZS (for DS3) or HDB3 (for E3). Therefore, after powerup, the encoder/decoder in either the framer or LIU must be turned off. Note that in Raw mode, encoding must be done by the LIU. (Decoding may be done in the framer or LIU.)

The LIU's Loss of Signal (LOS) threshold level is controlled by software via bit 7 of the LIU Control and Status Registers (P1ICSR and P2ICSR). The state of this bit forces the state of LOSTHR input pin of the LIU, which in turn defines the threshold levels for the incoming signal. If the incoming signal drops below the thresholds, a LOS will be generated by the LIU. Note: The threshold levels vary depending if the LIU equalizer is enabled or disabled. Refer to the XRT73(L)00 data sheet for further details.

The LIU's Line Code Violation (LCV) pin is connected to the FPGA, which keeps a count in the P1LCR and P2LCR register (one for each port). There are also LCV Threshold registers for each port, which set the number of LCVs detected before an interrupt is generated.

Data loopback modes.

The XRT7300 supports three loopback modes: analog local loopback, digital local loopback, and remote loopback.

Analog Local Loopback

In this mode, the LIU ignores any signals at its RTIP and RRING input pins. The data sampled at the TPDATA and TNDATA inputs are output on the TTIP and TRING output pins and is looped back into the AGC/Equalizer block of the LIU. This data is then processed and sent out on the RPOS and RNEG output pins.

Digital Local Loopback

In this mode, the LIU again ignores any signals at its RTIP and RRING input pins. The data sampled at the TPDATA and TNDATA inputs are processed through the HDB3/B3ZS Encoder block and then looped back to the HDB3/B3ZS Decoder block where the data is sent out on the RPOS and RNEG output pins.

Remote Loopback

In this mode, the LIU ignores any signals at its TPDATA and TNDATA input pins. Data is received on the RTIP and RRING inputs, processed and output on the RPOS and RNEG output pins. This data is also internally looped back into the Pulse-Shaping block, processed and set out onto the TTIP and TRING output pins.

T3/E3 magnetics

For each port, two types of magnetics are used: an isolation transformer and a common-mode choke. The isolation transformer selected is a dual module that has two 1:1 transformers, one is used for transmit side and the other for receive side. The dual isolation module is a HALO TG01-0406N1 in a 16-pin surface mount N1 package.

The common-mode choke is a triple module that has three common-mode chokes; one is used for each TIP/RING signal pair. Each choke has a winding resistance of 200 milliohms. The module is a Pulse 23Z106SM in a 16-pin surface mount package. Note: The chokes must be placed as close as possible to the BNC connectors.

T3/E3 connector

Two BNC connectors are used for each port, one for the transmit signal and the other for receive. The shield of the BNC connector is electrically connected to the bezel. Special board cut-outs are required to accommodate the hardware which attaches the connector to the bezel. Trace impedances between the LIU and connectors should be controlled as close to 75 ohms as possible.

Pn4 connector option

IDT's Quick Switch QS3VH257Q is used to route the LIU line-side signals to either the on-board transformers/common-mode chokes for front panel I/O or to the Pn4 connector for rear panel I/O. The TIP/RING signal pairs from the Quick Switch devices to Pn4 are routed as differential pairs on internal board layers. The impedance of the traces are controlled to 75 ohms for transmit signals, and 100 ohms for receive signals. Extra clearance is provided for the traces to reduce crosstalk susceptibility. (See connectors)

Digital-to-Analog Converter(Optional)

A 12-bit Digital-to-Analog Converter (DAC) is used to supply a programmable voltage level to a voltage-controlled crystal oscillator (VCXO) to provide a pullable clock option. The DAC, a Texas Instrument's TLV5636 in an 8-pin plastic SOIC package, is programmed through its 3-wire serial interface (CLK and DIN via the serial I/O bus, and CS via the SCSR register) using a 16-bit serial string. The 16-bit string is broken into two parts: four bits for program (D15:D12) and 12 bits for data (D11:D0). Depending on the value of the program bits, the software can either write to the DAC register or to the Control register.

Pullable clock scheme

There are two separate oscillator control circuits; one for each port. Each circuit has a DAC and a VCXO. A VCXO centered at 44.736MHz is used for T3 applications and one centered at 34.368MHz is used for E3 applications. Both VCXOs selected are Vectron International's VCUJCA, a 5-volt VCXO with an absolute pull range of +/- 50 PPM in a 6-pin ceramic LCC package. When programmed to use its own 2.048V internal reference, the TLV5636 has an output range of 0 volt to 4.095 volts (DAC data value range from 000 hex to FFF hex) in 1-millivolt increments. The VCXO's input voltage range is 0.5 volt to 4.5 volts, which translates into a "pull" of -50 PPM to +50 PPM of the center frequency. Two 1-Kohm potentiometers are implemented to guarantee that the VCXOs on each product produce the same frequency (within an acceptable tolerance) for a given data value in the DACs. In other words, the potentiometers allow for offset and gain control to ensure the same slope from product to product.

Modes of Operation

There are three modes of operation: HDLC mode, transparent mode, and raw mode. Two of the modes (HDLC and transparent) are considered payload modes because they deal only with the payload data fields of the DS3 frame. Whereas in the raw mode, both the overhead bit fields and payload data fields of the DS3 frame are used.

HDLC mode

In HDLC mode, all the bits of the HDLC frame after zero-bit insertion, as well as the flag bits between frames, are located in the payload data field of the DS3 frame. The transmitter continuously sends flags until data is available to be transmitted. Flags may be shared, that is, only one flag between two frames of data. The OSS-wanPMC-xT3E3 transmits a minimum of one flag between HDLC frames by default. The FCNT bits in the Port n Control Register B can be set to change the minimum number of flags. Note: For every Ethernet packet, there is one HDLC frame. Therefore, in 32-bit CRC HDLC mode the 32-bit CRC from the transmit

Ethernet packet can be appended to the end of the transmit HDLC frame prior to the zero-bit insertion process. For the incoming frame, the 32-bit CRC of the receive HDLC frame can be appended to the end of the receive Ethernet packet.

Transparent mode

In Transparent mode, the payload data field of the DS3 frame is considered as data only. Therefore HDLC processing is not required in this mode. Note: In this mode, CRC is disabled in the Ethernet controller.

Transmitter. If an Ethernet packet is ready to be transmitted, then the data is placed in the DS3/E3 payload data field, synchronized with the first frame pulse. For proper operation with the selected framing format, the Ethernet packet length must be fixed at 588 bytes (DS3 format), 190 bytes (E3 G.751 format with BIP-4 enabled), 191 bytes (E3 G.751 format with BIP-4 disabled), or 530 bytes (E3 G.832 format). The most significant nibble of the last byte of the 191-byte Ethernet packet is truncated because the actual E3 G.751 payload is 190.5 bytes per frame with the BIP-4 transmitter disabled.

If an Ethernet packet is not ready to be transmitted, then the payload data field is stuffed with a repeating data byte pattern determined by the value in the Payload Fill Register.

Receiver. The payload data field of each incoming DS3/E3 frame is transferred to the Ethernet controller as a single packet of data. Therefore, in Transparent mode, the Ethernet controller receive descriptors must be set up for the appropriate packet size (588, 190, 191, or 530 bytes). The last byte of the 191-byte E3 G.751 packet contains duplicate nibbles, one of which is not interpreted as received data.

Raw mode

In Raw mode, the overhead bit fields and the payload data fields of the DS3 frame are both considered as data. In this mode, CRC is also disabled in the Ethernet controller. Note: In this mode, both the Framer and LIU must be set for Unipolar signaling rather than the default of Bipolar signaling. To accomplish this, the Unipolar bit in the Framer I/O Control Register is set to "1" along with the TXBIN and RNRZ bits in the LIU Command Registers.

Transmitter. If an Ethernet packet is ready, then the overhead bit field and payload data fields are stuffed with data. For proper operation with the selected framing format, the Ethernet packet length must be fixed at 595 bytes (DS3 format), 192 bytes (E3 G.751 format), or 537 bytes (E3 G.832 format). If an Ethernet packet is not ready, then the DS3/E3 framer is allowed to generate the framing bits and the payload data field is stuffed with a repeating data byte pattern determined by the value in the Payload Data Register.

Receiver. All the payload and framing bits from a single DS3/E3 frame are transferred to the Ethernet controller as a single packet. Therefore, the Ethernet controller receive descriptors must be set up for the appropriate packet size (595, 192, or 537 bytes).

Connectors

Pn1 32-bit PCI				Pn2 32-bit PCI				Pn4 I/O (Optional)			
Pin #	Name	Name	Pin #	Pin #	Name	Name	Pin #	Pin #	Name	Name	Pin #
1	TCK	-12V	2	1	+12V	TRST#	2	1	TTIP1_PN4	TRING1_PN4	2
3	Ground	INTA#	4	3	TMS	TDO	4	3	No Connect	No Connect	4
5	INTB#	INTC#	6	5	TDI	Ground	6	5	No Connect	No Connect	6
7	BUSMODE1#	+5V	8	7	Ground	PCI-RSVD	8	7	No Connect	No Connect	8
9	INTD#	PCI-RSVD	10	9	PCI-RSVD	PCI-RSVD	10	9	RTIP1_PN4	RRING1_PN4	10
11	Ground	3.3Vaux	12	11	BUSMODE2#	+3.3V	12	11	No Connect	No Connect	12
13	CLK	Ground	14	13	RST#	BUSMODE3#	14	13	No Connect	No Connect	14
15	Ground	GNT#	16	15	+3.3V	BUSMODE4#	16	15	No Connect	No Connect	16
17	REQ#	+5V	18	17	PME#	Ground	18	17	TTIP2_PN4	TRING2_PN4	18
19	V(I/O)	AD[31]	20	19	AD[30]	AD[29]	20	19	No Connect	No Connect	20
21	AD[28]	AD[27]	22	21	Ground	AD[26]	22	21	No Connect	No Connect	22
23	AD[25]	Ground	24	23	AD[24]	+3.3V	24	23	No Connect	No Connect	24
25	Ground	C/BE[3]#	26	25	IDSEL	AD[23]	26	25	No Connect	/LED1AY	26
27	AD[22]	AD[21]	28	27	+3.3V	AD[20]	28	27	/LED1AG	No Connect	28
29	AD[19]	+5V	30	29	AD[18]	Ground	30	29	RTIP2_PN4	RRING2_PN4	30
31	V(I/O)	AD[17]	32	31	AD[16]	C/BE[2]#	32	31	No Connect	No Connect	32
33	FRAME#	Ground	34	33	Ground	PMC-RSVD	34	33	No Connect	No Connect	34
35	Ground	IRDY#	36	35	TRDY#	+3.3V	36	35	No Connect	/LED2AY	36
37	DEVSEL#	+5V	38	37	Ground	STOP#	38	37	/LED2AG	/LED3AY	38
39	Ground	LOCK#	40	39	PERR#	Ground	40	39	/LED3AG	/LED4AY	40
41	PCI-RSDV*	PCI-RSVD	42	41	+3.3V	SERR#	42	41	No Connect	No Connect	42
43	PAR	Ground	44	43	C/BE[1]#	Ground	44	43	/LED4AG	No Connect	44
45	V(I/O)	AD[15]	46	45	AD[14]	AD[13]	46	45	No Connect	/LED1BY	46
47	AD[12]	AD[11]	48	47	M66EN	AD[10]	48	47	/LED1BG	/LED2BY	48
49	AD[09]	+5V	50	49	AD[08]	+3.3V	50	49	/LED2BG	/LED3BY	50
51	Ground	C/BE[0]#	52	51	AD[07]	PMC-RSVD	52	51	/LED3BG	/LED4BY	52
53	AD[06]	AD[05]	54	53	+3.3V	PMC-RSVD	54	53	/LED4BG	No Connect	54
55	AD[04]	Ground	56	55	PMC-RSVD	Ground	56	55	No Connect	No Connect	56
57	V(I/O)	AD[03]	58	57	PMC-RSVD	PMC-RSVD	58	57	No Connect	No Connect	58
59	AD[02]	AD[01]	60	59	Ground	PMC-RSVD	60	59	No Connect	No Connect	60
61	AD[00]	+5V	62	61	ACK64#	+3.3V	62	61	No Connect	No Connect	62
63	Ground	REQ64#	64	63	Ground	PMC-RSVD	64	63	No Connect	No Connect	64